1974-12

Design optimization of metal-insulator-semiconductor devices for infrared solid state imaging

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DESIGN OPTIMIZATION OF METAL-INSULATOR-SEMICONDUCTOR DEVICES FOR INFRARED SOLID STATE IMAGING

Numa Augustine Boudreaux

NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

DESIGN OPTIMIZATION OF METAL-INSULATOR-SEMICONDUCTOR DEVICES
FOR
INFRARED SOLID STATE IMAGING

by

Numa Augustine Boudreaux III

December 1974

Thesis Advisor: T.F. Tao

Approved for public release; distribution unlimited.

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle)

Design Optimization of Metal-Insulator-Semiconductor Devices for Infrared Solid State Imaging

5. TYPE OF REPORT & PERIOD COVERED

Master's Thesis; December 1974

6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s)

Numa Augustine Boudreaux III

8. CONTRACT OR GRANT NUMBER(s)

9. PERFORMING ORGANIZATION NAME AND ADDRESS

Naval Postgraduate School
Monterey, California 93940

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS

11. CONTROLLING OFFICE NAME AND ADDRESS

Naval Postgraduate School
Monterey, California 93940

12. REPORT DATE

December 1974

13. NUMBER OF PAGES

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)

Naval Postgraduate School
Monterey, California 93940

15. SECURITY CLASS. (of this report)

Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Infrared Imaging, M-I-S, CCD, and CID

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

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S/N 0102-014-6601 |

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

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Design Optimization of Metal-Insulator-Semiconductor Devices

for

Infrared Solid State Imaging

by

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Submitted in partial fulfillment of the
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MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL

December 1974

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This study provides a methodology for design optimization of metal-insulator-semiconductor device utilized as charge storage infrared detectors. A new general formulation for the calculation of efficient charge storage capacity is derived and compared to existing formulas. Design parameter constraints are examined and several performance improvement techniques are discussed. A new device structure is proposed which integrates many desirable features into a single element. The results of this study indicate that the trend should be toward charge injection devices constructed of p-type group IV-VI thin film semiconductors with high dielectric constant insulators using back-illumination through anti-reflection layers.

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A	Absorptance
C	Total Capacitance
C_D	Space Charge Capacitance
C_{DD}	M-I-S Deep Depletion Capacitance
$C_{HF\ INV}$	M-I-S High Frequency Inversion Capacitance
C_i	Insulator Capacitance
C_{INV}	M-I-S Inversion Capacitance
C_{MIN}	M-I-S Minimum Capacitance
D	Diffusion Coefficient
E_c	Energy of Lower Edge of Conduction Band
E_g	Band Gap Energy
E_i	Intrinsic Fermi Level Engergy
E_v	Energy of Upper Edge of Valence Band
J_{DARK}	Dark Current Density
J_{FD}	Current Density due to Fabrication Defects
J_{GB}	Current Density due to Generation in the Bulk
J_{GD}	Current Density due to Generation in the Depletion Region
J_{SS}	Current Density due to Surface States
J_T	Current Density due to Tunneling

ℓ	CCD Intercell Distance
ℓ	Linear Thermal Expansion Coefficient
L	Diffusion Length
L_D	Extrinsic Debye Length
n	Electron Concentration
n	Index of Refraction
n_i	Intrinsic Carrier Concentration
n_o	Electron Concentration in the Bulk
n_s	Electron Concentration at the Surface
N	Doping Level
N_A	Acceptor Concentration
N_D	Donor Concentration
N_{MAX}	Maximum Density of Stored Carriers
p	Hole Concentration
p_o	Hole Concentration in the Bulk
p_s	Hole Concentration at the Surface
Q_B	Background Photon Flux Density
Q_{DEP}	Charge in the Depletion Region
Q_{FC}	Fixed Charge in the Insulator
Q_{INV}	Charge in the Inversion Layer
Q_{INVI}	Initial Charge in the Inversion Layer
Q_{INVF}	Final Charge in the Inversion Layer
Q_m	Charge on the Metal Gate

Q_s	Charge in the Semiconductor
Q_{ss}	Charge in the Surface States
R	Reflectance
R	Total Resistance
R_m	Metal Resistance
R_s	Semiconductor Resistance
S_o	Surface Recombination Velocity
V_g	Gate Voltage
V_i	Voltage Across the Insulator
V_T	Gate Voltage at Threshold of Inversion
W	Depletion Region Width
W_{MAX}	Maximum Depletion Region Width
z	Parameter to Determine Quantum Efficiency

GREEK LETTERS

α	Absorption Coefficient
ε_i	Permitivity of Insulator
ε_o	Permitivity of Free Space
ε_s	Permitivity of Semiconductor
η	Quantum Efficiency
κ_i	Insulator Relative Dielectric Constant
κ_s	Semiconductor Relative Dielectric Constant
μ_m	Minority Carrier Mobility

t_{GR}	Generation-Recombination Lifetime
τ_{id}	Dark Integration Time
τ_m	Minority Carrier Lifetime
τ_{tr}	Transfer Time
ϕ_m	Metal Work Function
ϕ_{ms}	Metal-Semiconductor Work Function
χ	Semiconductor Electron Affinity
Ψ_B	Potential Difference Between Fermi Level and Intrinsic Fermi Level
Ψ_s	Surface Potential

I. INTRODUCTION

A. SOLID STATE INFRARED IMAGING

The development of solid state devices for imaging applications is nearly as old as solid state electronics itself. Discrete component photo-conductive and photo-voltaic devices were fabricated and employed with various scanning schemes to produce scene images. The advent of large scale integration (LSI) technology provided a vehicle for production of multi-element detector arrays which stimulated imaging researchers into thoughts of large nonscanned staring solid state imagers. Linear arrays of detectors were fabricated which performed well but the progression to staring arrays was stymied by the problems of interconnecting all the elements of a large staring array. The discovery of the Charge Coupled Device (CCD) [2] created excitement in the imaging field since it potentially offered a method to solve the interconnection problem and "The Solid State Imaging Revolution" was underway [8]. Owing to the very advanced state of silicon technology, most of the early work was in the visible spectrum and a few companies are now marketing Charge Transfer Device (CTD) arrays of moderate size. Since the potential commercial market for these devices is immense, interest is high and competition is keen. The progress of infrared solid state imaging (IRSSI) has not kept pace with

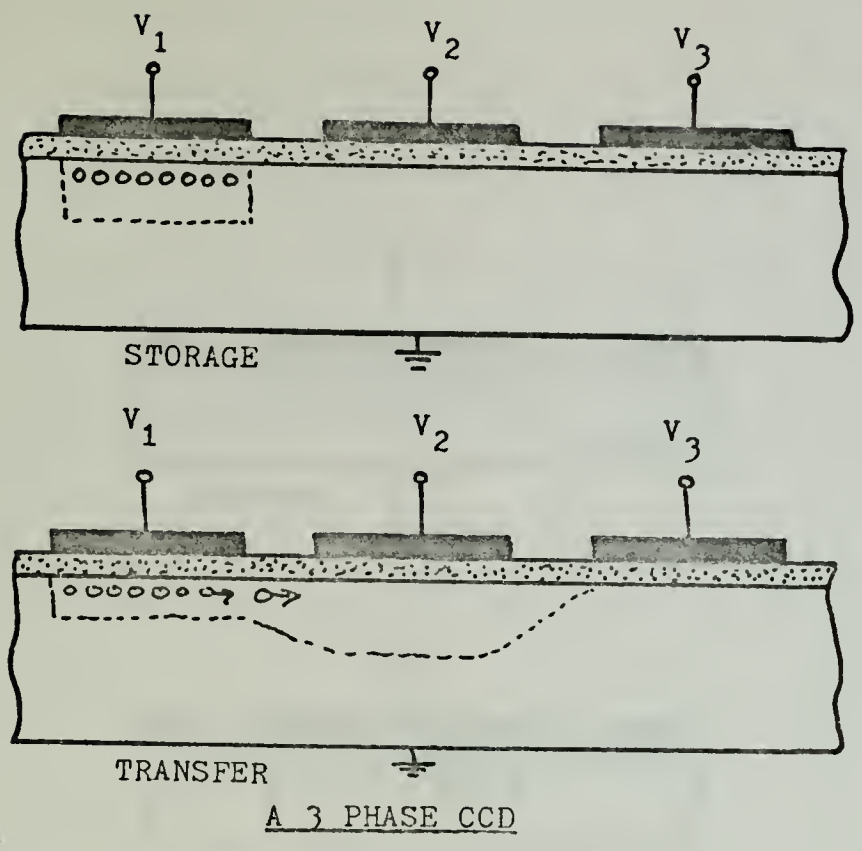
visible imaging because the potential market is smaller, scene background radiation levels are high, and narrow-gap semiconductor technology is much less advanced than silicon. Nevertheless, there are some notable pioneering efforts underway to develop charge transfer devices for IRSSI [1] [15] [16] [17] [24] [25] [28] [29].

B. CHARGE TRANSFER DEVICE PRINCIPLES

The basic CTD principle consists of storage and transfer of charge "packets," containing signal information, within metal-insulator-semiconductor (M-I-S) structures. It must be emphasized that the operation consists of two distinct events: storage and transfer. Minority or majority carriers may be stored depending on whether the device is operated in the depletion or accumulation mode. The transfer of charge may be accomplished by coupling action between M-I-S structures (Charge Coupled Devices) or by injection action into the substrate (Charge Injection Devices).

1. Charge Coupled Devices

CCD operation consists of storing minority carriers in potential wells created in the semiconductor near its interface with the insulator, and moving these charges as a unit into an adjacent similar device by varying gate voltages. A typical three-phase pulse sequence CCD operation is illustrated in Figure 1.



A 3 PHASE CCD

Figure 1

2. Charge Injection Devices

CID operation consists of storing minority carriers as in the CCD. Transfer is accomplished by reducing the gate voltage to a lower value which will inject the stored charge into the substrate. The recombination of the injected minority carriers with majority carriers in the substrate creates a current in the external circuit which is proportional to the stored charge. A typical sequence is shown in Figure 2.

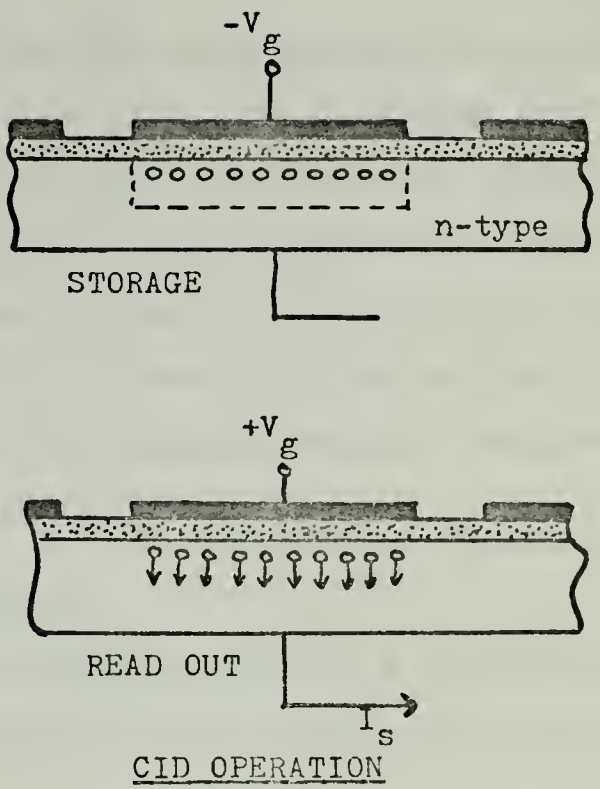


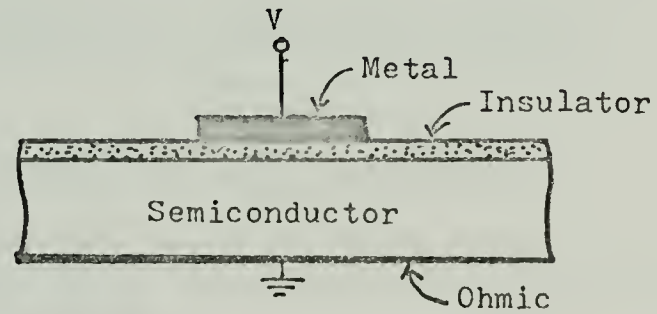
Figure 2

II. METAL-INSULATOR-SEMICONDUCTOR THEORY

The MIS structure was first proposed as a voltage variable capacitor in 1959 [27]. These devices were found to be useful as vehicles to study semiconductor surfaces and a new technology was born. For completeness, the ideal MIS device is first considered followed by a discussion of the non-ideal mechanisms. This is followed by a new approach to the formulation of equations designed to describe the dynamic performance parameters.

A. IDEAL MIS PHYSICS

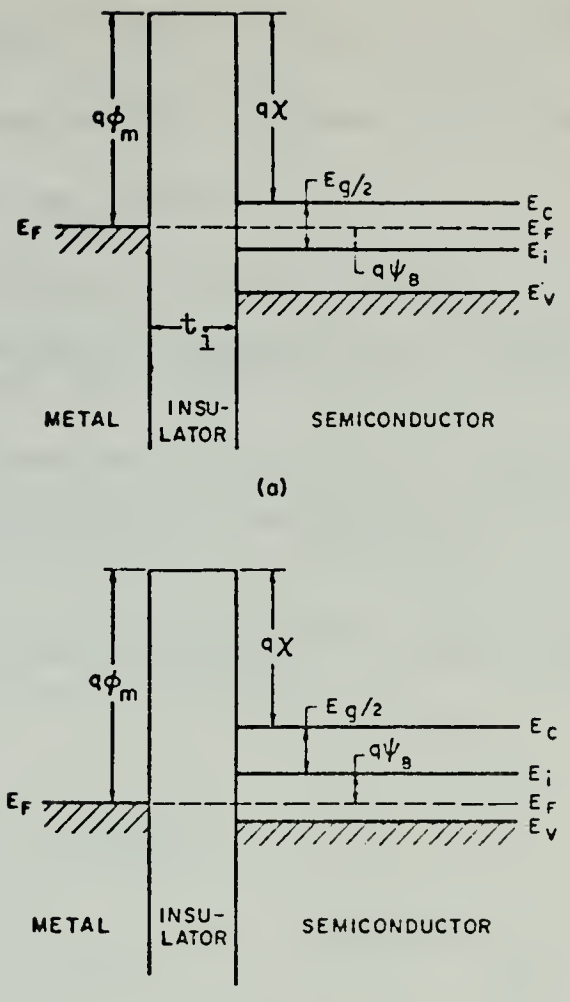
The basic MIS device consists of a semiconductor layer covered by an insulator layer onto which a metal electrode is deposited.



IDEAL M-I-S STRUCTURE

Figure 3

The energy band diagram of an ideal MIS device is shown in Figure 4.



IDEAL M-I-S ENERGY BAND DIAGRAM

Figure 4

An ideal MIS diode is defined as follows:

1. At zero applied bias there is no energy difference between the metal work function and the semiconductor work function, or

$$\phi_{ms} = \phi_m - (\chi + \frac{Eg}{2q} - \Psi_B) = 0 \text{ for n-type}$$

$$\phi_{ms} = \phi_m - (\chi + \frac{Eg}{2q} + \Psi_B) = 0 \text{ for p-type}$$

where ϕ_m = metal work function

χ = semiconductor electron affinity

E_c = energy of the lower edge of the conduction band

E_v = energy of the upper edge of the valence band

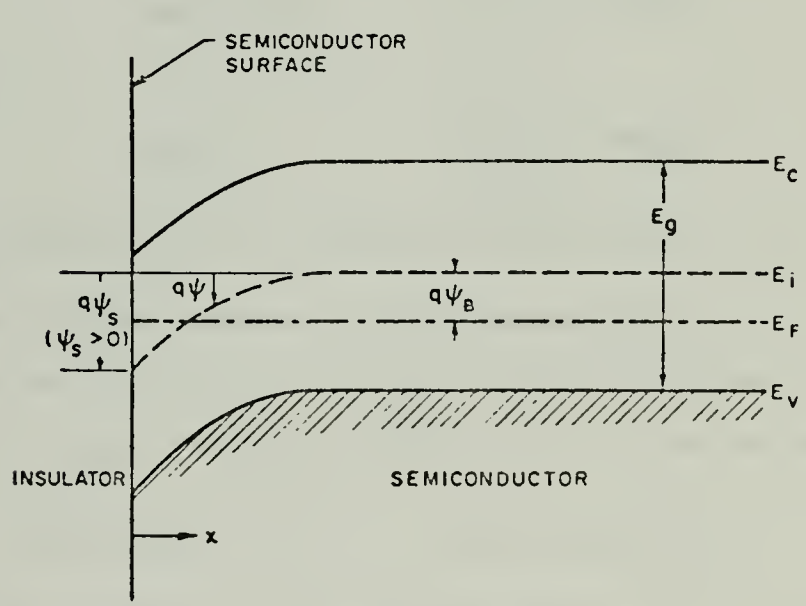
E_g = band gap energy

q = elementary electronic charge

Ψ_B = potential difference between the Fermi level E_F and the intrinsic Fermi level E_i

2. The only charges that can exist in the structure under any biasing conditions are those in the semiconductor and those with equal but opposite sign on the metal surface adjacent to the insulator.

3. There is no carrier transport through the insulator under dc biasing conditions, or the resistivity of the insulator is infinite.



IDEAL M-I-S SURFACE ENERGY BAND DIAGRAM

Figure 5

Figure 5 shows the band diagram at the surface of a p-type crystal. A positive voltage at the field plate causes

the bands to be bent downward. Each energy level can be associated with a potential Ψ by dividing by the elementary charge q.

$$q\Psi = -E_i$$

It is convenient to chose the origin of the potential so that it is zero in the bulk. The bands are flat in the bulk semiconductor except at the surface where surface fields can cause band bending. The Fermi level, which is the electrochemical potential, depends only on the properties of the crystal and remains fixed despite band bending.

Electron and hole concentrations are given by:

$$\text{electrons} \qquad n = n_o e^{q\Psi/kT}$$

$$\text{holes} \qquad p = p_o e^{-q\Psi/kT}$$

where n_o and p_o are the respective densities of the electrons and holes in the interior of the semiconductor; k is the Boltzmann constant; and T is the absolute temperature.

At the surface of the crystal, the concentrations are

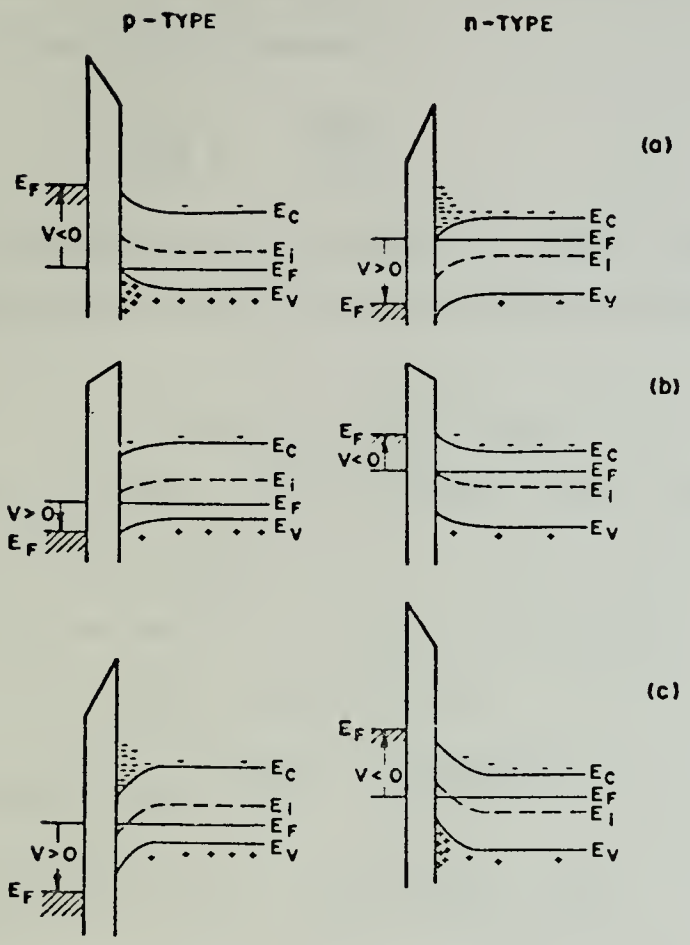
$$n_s = n_o e^{q\Psi_s/kT} \qquad p_s = p_o e^{-q\Psi_s/kT}$$

where the subscript s refers to quantities at the surface.

The following ranges of surface potential can be distinguished for p-type (see left side of Figure 6):

1. $\Psi_s < 0$ Enhanced hole concentration-accumulation layer
2. $2\Psi_B > \Psi_s > 0$ Depleted hole concentration-depletion layer

3. $\Psi_s > 2\Psi_B$ Electron enhancement-inversion layer



IDEAL M-I-S ENERGY BAND DIAGRAM

Figure 6

For n-type (right side of Figure 6), the same definitions apply for the opposite direction of band bending. In addition two specific values of surface potential are important:

1. $\Psi_s = 0$ Flat-band condition

2. $\Psi_s = \Psi_B$ Midgap with $n_s = p_s = n_i$

The electrostatic potential in the semiconductor and the space charge $\rho(x)$ are related by the Poisson equation (assuming one-dimensional geometry):

$$\frac{d^2\psi}{dx^2} = - \frac{\rho(x)}{\varepsilon_s}$$

where ε_s is the dielectric permittivity of the semiconductor; $\rho(x)$ is the algebraic sum of all the charge densities in the crystal

$$\rho = q(N_D - N_A + p - n)$$

where N_D and N_A represent the densities of the ionized donors and acceptors respectively.

In the bulk we have $\psi = 0$ and $\rho = 0$, and so

$$N_D - N_A = n_o - p_o$$

then $\rho = q(n_o - p_o + p_o e^{-q\psi/kT} - n_o e^{q\psi/kT})$

$$= q\left[p_o(e^{-q\psi/kT} - 1) - n_o(e^{q\psi/kT} - 1)\right]$$

The one-dimensionsal Poisson equation is then

$$\frac{d^2\psi}{dx^2} = - \frac{q}{\varepsilon_s}\left[p_o(e^{-q\psi/kT} - 1) - n_o(e^{q\psi/kT} - 1)\right]$$

Integration from the bulk toward the surface yields

$$\int_o^{\frac{\partial\psi}{\partial x}} \left[\frac{\partial\psi}{\partial x}\right] d\left[\frac{\partial\psi}{\partial x}\right] = - \frac{q}{\varepsilon_s} \int_o^{\psi} \left(p_o(e^{-q\psi/kT} - 1) - n_o(e^{q\psi/kT} - 1)\right) d\psi$$

since $\mathcal{E} = - \frac{\partial\psi}{\partial x}$

$$\mathcal{E} = \left\{ \left(\frac{2kT}{q} \right)^2 \left(\frac{q^2 p_o}{2\varepsilon_s kT} \right) \left[\left(e^{-q\Psi/kT} + \frac{q\Psi}{kT} - 1 \right) + \frac{n_o}{p_o} \left(e^{q\Psi/kT} - \frac{q\Psi}{kT} - 1 \right) \right] \right\}^{1/2}$$

for clarity let

$$F\left[\frac{q\Psi}{kT} , \frac{n_o}{p_o} \right] = \left[\left(e^{-q\Psi/kT} + \frac{q\Psi}{kT} - 1 \right) + \frac{n_o}{p_o} \left(e^{q\Psi/kT} - \frac{q\Psi}{kT} - 1 \right) \right]^{1/2}$$

The extrinsic Debye length, $L_D = \left(\frac{2kT\varepsilon_s}{p_o q^2} \right)^{1/2}$

$$\mathcal{E} = \pm \frac{2kT}{qL_D} F \left[\frac{q\Psi}{kT} , \frac{n_o}{p_o} \right]$$

which is + for $\Psi > 0$ and - for $\Psi < 0$.

The electric field at the surface, $\mathcal{E}_s$, is then

$$\mathcal{E}_s = \pm \frac{2kT}{qL_D} F \left[\frac{q\Psi_s}{kT} , \frac{n_o}{p_o} \right]$$

By Gauss' Law the space charge per unit area required to produce this field is

$$Q_s = \varepsilon_s \mathcal{E}_s = \mp \frac{2 \varepsilon_s kT}{q L_D} F \left[\frac{q\Psi_s}{kT} , \frac{n_o}{p_o} \right]$$

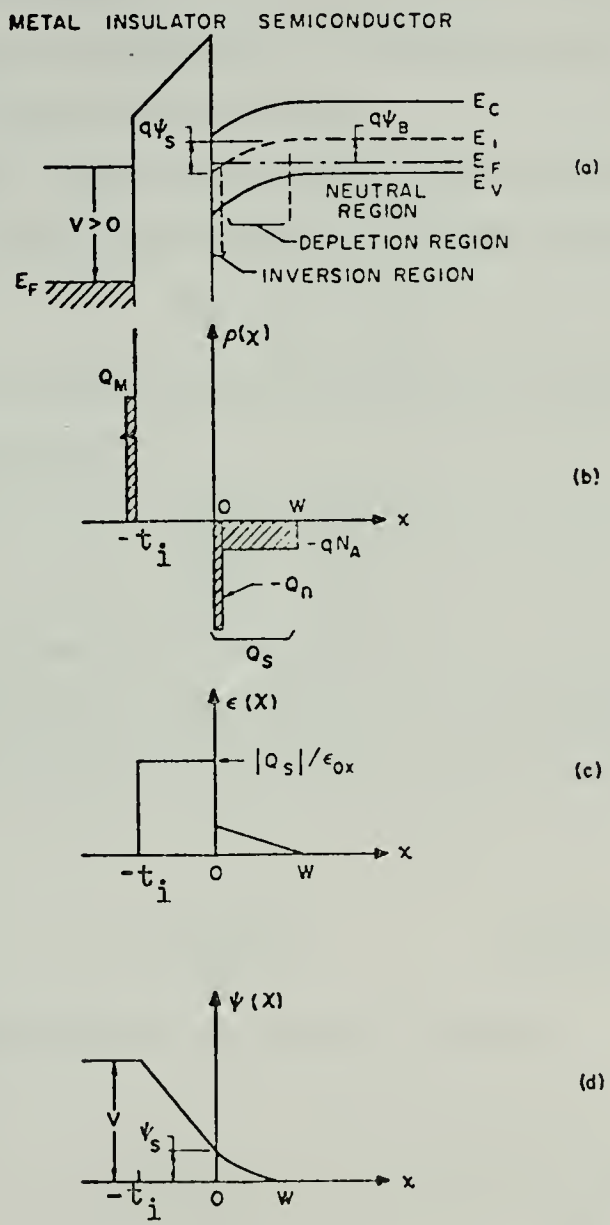
The differential capacitance of the semiconductor space-charge region is

$$C_D = \frac{\partial Q_s}{\partial \Psi_s} = \frac{\varepsilon_s}{L_D} \frac{\left[1 - e^{-q\Psi_s/kT} + \frac{n_o}{p_o} \left(e^{q\Psi_s/kT} - 1 \right) \right]}{F\left[\frac{q\Psi_s}{kT} , \frac{n_o}{p_o} \right]} \quad \text{farad/cm}^2$$

At flat-band, $\Psi_s = 0$ and

$$C_D \text{ (flat band)} = \frac{\sqrt{2}\,\varepsilon_s}{L_D} \quad \text{farad/cm}^2$$

Figure 7 shows the band diagram of an ideal MIS structure with p-type semiconductor



IDEAL M-I-S ELECTRICAL DISTRIBUTIONS

Figure 7

For charge neutrality of the system

$$Q_m = Q_{inv} + q\,N_A\,W = Q_s$$

where Q_m is charges per unit area on the metal, Q_{inv} is the electrons per unit area in the inversion region, $q\,N_A\,W$ is the ionized acceptors per unit area in the space-charge region with space-charge width W, and Q_s is the total charges per unit area in the semiconductor.

In the ideal case the applied voltage will partly appear across the insulator and partly across the semiconductor.

$$V_g = V_i + \Psi_s$$

where V_g is the applied voltage and V_i is the potential across the insulator

$$V_i = \frac{Q_s}{C_i} = \frac{Q_s t_i}{\varepsilon_i}$$

where t_i is the insulator thickness.

The total capacitance of the device, C, is the series combination of the insulator capacitance and the space-charge capacitance

$$C = \frac{C_i\,C_D}{C_i + C_D} \qquad \text{farads/cm}^2$$

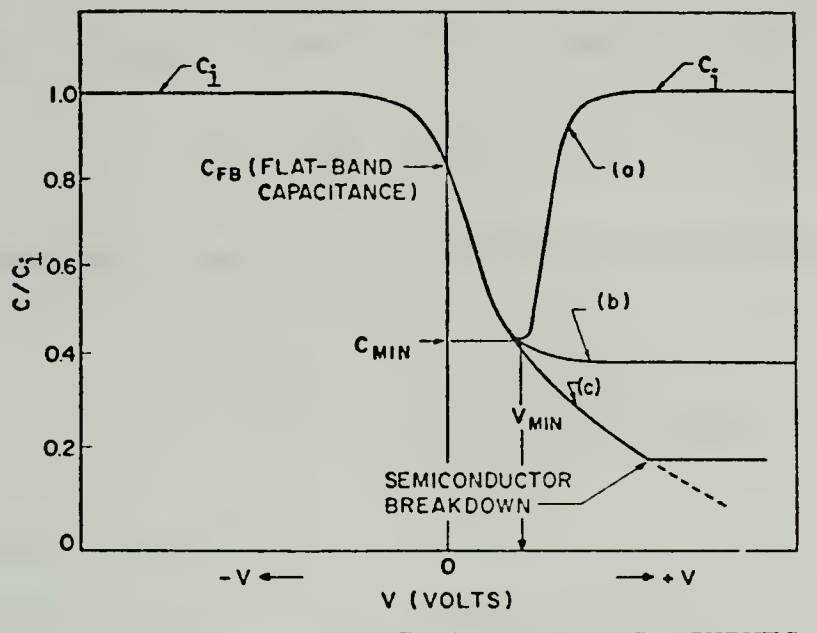
The total capacitance at flat-band is then

$$C_{FB}\ (\Psi=0) = \frac{\varepsilon_i}{t_i + \frac{1}{\sqrt{2}}\left(\frac{\varepsilon_i}{\varepsilon_s}\right) L_D} = \frac{\varepsilon_i}{t_i + \frac{\varepsilon_i}{\varepsilon_s}\sqrt{\frac{kT\varepsilon_s}{p_o\,q^2}}} \qquad \text{farads/cm}^2$$

A plot of the normalized total capacitance of the device

$$\frac{C}{C_i} = \frac{C_D}{C_i + C_D}$$

for a range of applied voltage is shown in Figure 8.



IDEAL M-I-S CAPACITANCE-VOLTAGE CURVES

Figure 8

Integration of Poisson's equation yields the potential distribution in the depletion region

$$\Psi = \Psi_s \left(1 - \frac{x}{w}\right)^2$$

where $\Psi_s = \frac{qN_A W^2}{2\,\varepsilon_s}$

then the maximum depletion width

$$W_{max} = \left(\frac{2\,\varepsilon_s\,\Psi_s}{q\,N_A}\right)^{1/2}$$

For steady state operation the onset of strong inversion occurs at $\Psi_s = 2\Psi_B$ and the depletion approximation may be obtained

$$W_{max} \simeq \left(\frac{2\varepsilon_s \psi_{s_{inv}}}{q N_A} \right)^{1/2} = \left[\frac{4\varepsilon_s kT \ln\left(\frac{N_A}{n_i}\right)}{q^2 N_A} \right]^{1/2}$$

The applied voltage at which strong inversion occurs is

$$V_T = \frac{Q_s}{C_i} + 2\psi_B$$

and the corresponding device capacitance is given by

$$C_{inv} = \frac{\varepsilon_i}{t_i + \left(\frac{\varepsilon_i}{\varepsilon_s} \right) W_{max}}$$

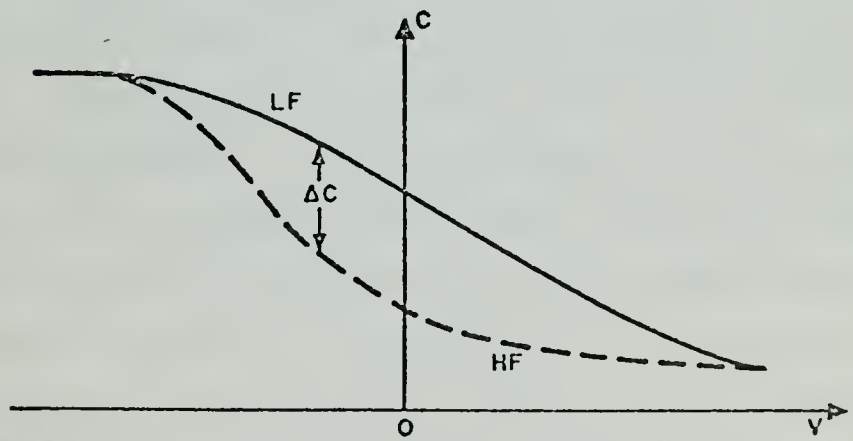
B. NON-IDEAL MECHANISMS

The fabrication of M-I-S devices and the physical parameters of the materials involved introduce factors that cause deviations from ideal behavior. To predict device performance requires a knowledge of these factors and their influences. In some cases it may be that these deviations from ideal behavior enchance rather than degrade device performance. The most fundamental non-ideal mechanisms are discussed below.

1. Interface States

An interface state is defined as an allowed energy level within the forbidden gap at the surface. There are two types of interface states, namely donor states and acceptor states. A donor state can have two states of charge. It can be neutral, or it can become positive by giving up an electron. Its state of charge is controlled by

the Fermi level. It is in its more positive state when it is above the Fermi level. An acceptor state, conversely, changes its charge between neutrality and negative. When there is energy band bending produced by external bias, the surface state levels will move in consonance with the valence and conduction bands, while the Fermi level remains fixed. Charge interchange with surface states contributes to the M-I-S capacitance and alters the ideal curve. This alteration is indicated in Figure 9 and shows a threefold effect. Interface states can produce a change in device capacitance, cause a frequency dispersion, and shift the voltage axis by changing the dependence of the surface potential on the applied bias [27].



VARIATION IN C-V CURVE DUE TO INTERFACE STATES

Figure 9

2. Work Function

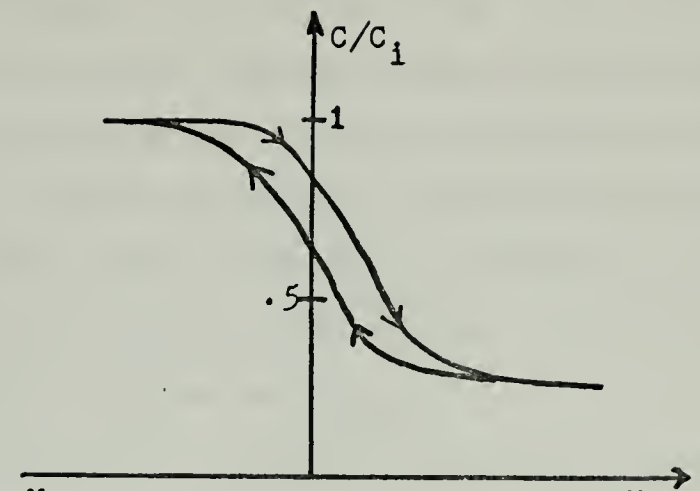
In the ideal device it was assumed that the metal-semiconductor work function was zero.

$$\phi_{ms} = \phi_m - (\chi + \frac{E_g}{2q} + \Psi_B) = 0$$

for p-type. Ψ_B is negative for n-type. For narrow gap semiconductors used in the infrared, $\frac{Eg}{2q} \pm \Psi_B$ is less than a few tenths of a volt and hence not particularly important. However, the quantity $(\phi_m - \chi)$ can be an appreciable fraction of a volt and can be an important consideration for low gate voltage applications. In passing it must be remembered that if a metal contact is made on the backside of the semiconductor there will be another metal-semiconductor work function to consider. This will be discussed later under Operation Improvement Techniques.

3. Charges in the Insulator

Normally there are two types of charges in the insulator, fixed charges and mobile ions, which result from fabrication processes. The fixed charges will terminate a portion of the electric field lines resulting from the applied bias and will produce a parallel voltage shift in the C-V curve. However, no distortion of the curve is introduced. The mobile ions will tend to follow the variation of the applied bias, but more slowly than the carriers. The result is a hysterisis effect to the curve as shown in Figure 10.



HYSTERESIS EFFECT

Figure 10

That is, a curve generated by a negative to positive sweep of the bias will differ from one generated with a positive to negative sweep.

4. Dark Current

In a charge storage device the dark current determines the absolute limit on storage time. There are five sources of dark current in an M-I-S device:

1. Generation of carriers via generation-recombination centers in the depletion region.
2. Generation of carriers via surface states at the insulator-semiconductor interface.
3. Diffusion of minority carriers out of the neutral region of the bulk.
4. Fabrication defects (metal precipitates, insulator pinholes, photolithographic defects, defective material, etc.)
5. Tunneling between bands.

In equation form the total dark current per unit area may be represented as $J_{Dark} = J_{GD} + J_{SS} + J_{GR} + J_{FD} + J_T$ where the right hand side represents dark current sources (1) through (5) respectively. For reversed biased depletion mode devices, J_T is not significant. Fabrication defects must be kept small or the device will experience many other problems, so in practice J_{FD} must be made insignificant. The bulk diffusion contribution, J_{GB}, may or may not be significant so it must be retained in the final expression.

$$J_{GD} = \frac{q\, n_i^2}{N\, \tau_m} \sqrt{\mu_m \frac{kT}{q} \tau_m}$$

Surface state generation can be appreciable if the surface recombination velocity S_o is high. Therefore, it will be retained even though it is desirable to minimize S_o.

$$J_{SS} = \frac{q\, n_i\, S_o}{2}$$

The generation-recombination centers in the depletion region are normally the most significant contributor to dark current since the interaction takes place in an electric field.

$$J_{GD} = \frac{q\, n_i\, W}{2\, \tau_{GR}}$$

where τ_{GR} is the generation-recombination lifetime in the depletion width W. For most practical purposes, then, the total dark current may be represented by

$$J_{Dark} = \frac{q\, n_i\, W}{2\, \tau_{GR}} + \frac{q\, n_i\, S_o}{2} + \frac{q\, n_i^2}{N\, \tau_m} \sqrt{\mu_m \frac{kT}{q} \tau_m}$$

C. CHARGE STORAGE

There are at least three different formulas in current literature for calculating the maximum charge storage capability of M-I-S devices.

$$N_{max} = (C_i - C_{min}) \frac{V_g}{q} = S2 \qquad \text{Ref. [17]}$$

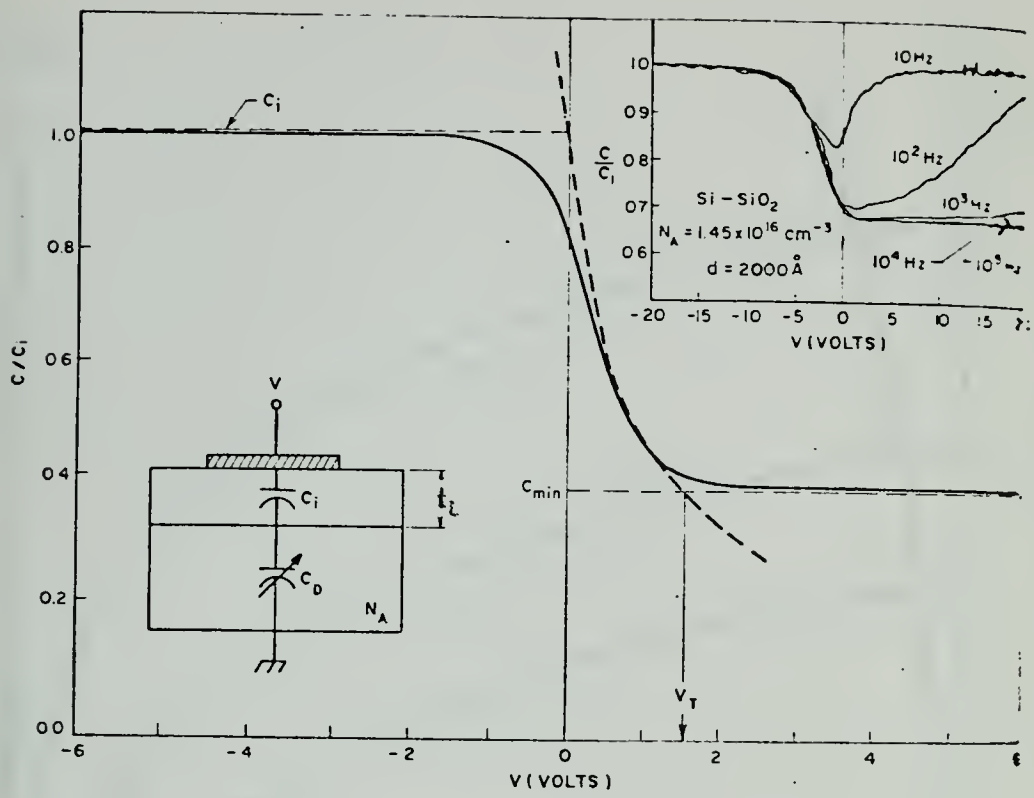
$$N_{max} = \frac{C_i}{q}(V_g - V_T) = S3 \qquad \text{Ref. [26]}$$

$$N_{max} = (C_{HF} - C_{DD}) \frac{V_g}{q} = S4 \qquad \text{Ref. [29]}$$
$$\text{INV}$$

Some mathematical and symbolic liberties have been taken to present the above formulas in a consistant format but the essence has been preserved. The parameters are defined as shown in Figure 11, and S2, S3, and S4 represent the computer program storage variables. A thorough examination of [17], [26], and [29] indicates that none of the formulas are expressly incorrect, but none are general enough to be universally applicable. A more general expression is derived, from the first principles of the device, in Appendix A.

$$N_{max} = \frac{Q_{INVF} - Q_{INVI}}{q}$$

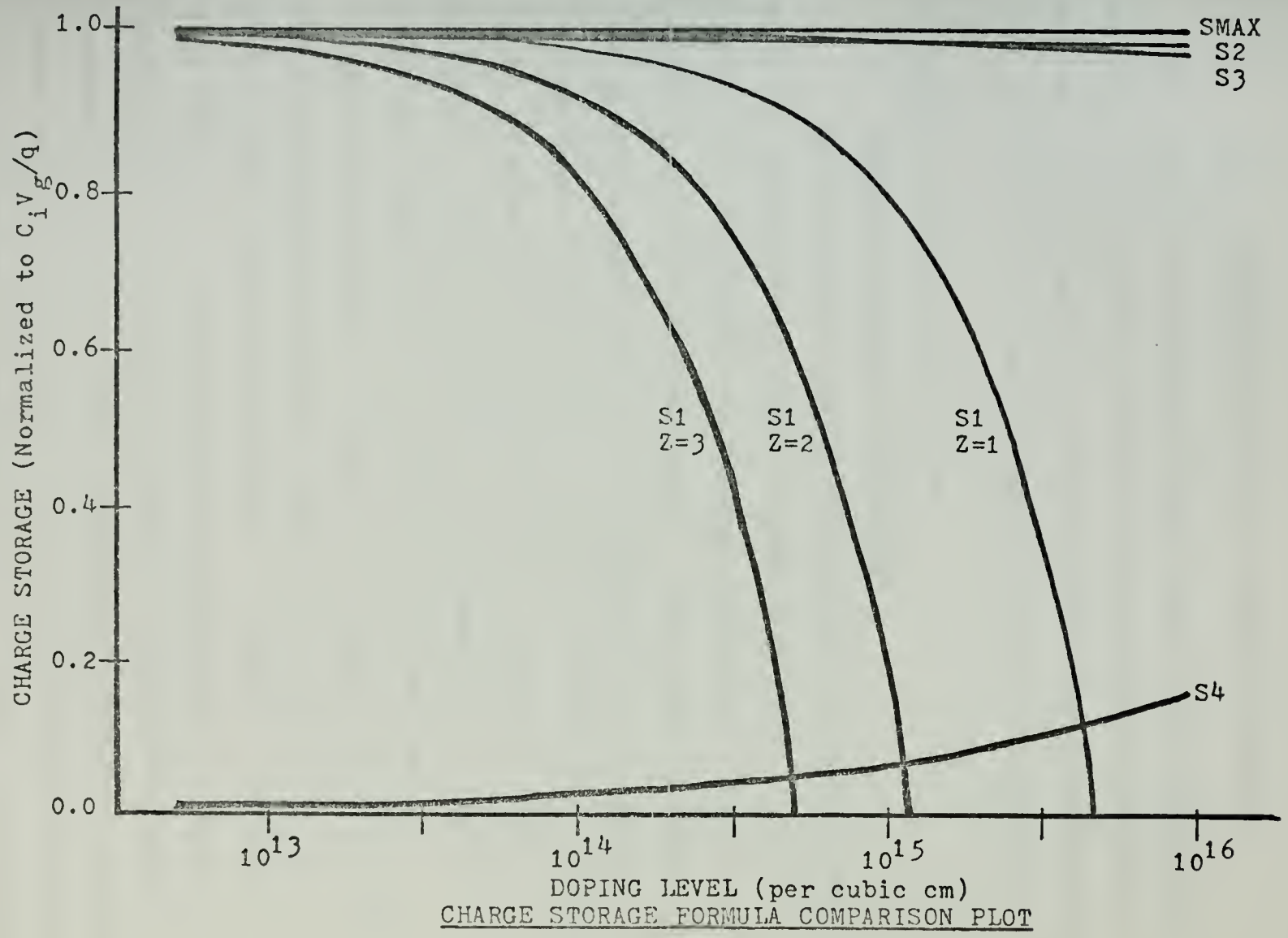
where Q_{INVF} and Q_{INVI} are the final and initial values of



HIGH FREQUENCY C-V CURVES

Figure 11

the charge stored in the inversion layer. A computer program was devised to compare all the charge storage formulas with the absolute maximum charge storage ($N_{max} = C_{INS} V_g/q$). The program is included in Appendix B and the comparative plot is shown in Figure 12.



CHARGE STORAGE FORMULA COMPARISON PLOT

Figure 12

III. CONSTRAINTS ON M-I-S DETECTOR DESIGN

All design is necessarily constrained by the availability, the inherent properties, and the interactions of materials to be used in the structure. In this section those considerations most important to the design engineer are briefly stated.

A. GENERAL PHYSICAL LIMITATIONS

1. Thermal Expansion Coefficients

The temperature variations resulting from processes needed in manufacture, normal storage techniques, and the operational environment can produce disasterous effects particularly on structured devices. These effects range from complete destruction due to rupturing of the contact at interfaces, to more subtle, but still undesirable, alterations of electrical properties when a crystal is under mechanical strain. Therefore, it is necessary to select materials whose thermal expansion coefficients are not drastically different. Of course, the larger the chip size and the greater the expected temperature variations, the more crucial this selection becomes. Generally, component size should be on the order of the wavelength so infrared components will be orders of magnitude larger than similar components used in the visible spectrum. Also since infrared photon energies are smaller, these detectors normally require cooling to reduce thermal generation. Normally this requires

that all thermal expansion coefficients at least be within the same order of magnitude.

2. Dielectric Strength

Although small voltages are normally associated with the operation of semiconductor devices, the small dimensions of device structures can produce large electric fields. These large fields and the normal existance of some degree of crystal defects can easily cause breakdown if dielectric strengths are not sufficiently large.

3. Resistivity

Ideally the insulator resistivity should be very large, the semiconductor resistivity very small, and the metal conductivity extremely large. Practically, however, there are limits as to how closely the ideal situation can be approached. Typical values for good quality material are:

Al	σ	$= 4X10^{5}$	mhos/cm
Al_2O_3	ρ	$= 2X10^{12}$	ohm-cm
InSb	ρ	$= 3$	ohm-cm ($N_A=2X10^{14}cm^{-3}$)

Experimental work has shown that some general conclusions may be made:

1. Insulator materials have sufficient resistivity to prevent any detrimental effects on device performance.
2. Metal conductivities are of no consequence when considering power dissipation but affect gate voltage pulse shape particularly in large arrays.
3. Semiconductor resistivities affect power dissipation and gate voltage pulse shape.

The verification of these general comments will be illustrated in Section V as part of the system calculation.

4. Power Dissipation

LSI fabricated circuits are limited as to the amount of average power which may be dissipated without material failure. Additionally, thermal power dissipation below failure levels can place great demands on the cooling system employed, and the device may actually be at a somewhat higher temperature than the cooling system. This will produce more thermal noise in the device which is certainly not desirable. The system calculation in section V illustrates the problem.

5. Dielectric Constant Relationship

In order to obtain a large storage capacity in a M-I-S structure it is necessary that there be a large variation in device capacitance. For an ideal device

$$C = \frac{C_i C_s}{C_i + C_s}$$

Normally the insulator thickness is on the order of a fraction of a micron while the depletion depth may be several microns. Typically they differ by about a factor of 50. Then as an approximation

$$C = \frac{\frac{\kappa_i}{t_i}\frac{\kappa_s}{t_s}}{\frac{\kappa_i}{t_i}+\frac{\kappa_s}{t_s}} \simeq \frac{\kappa_i \kappa_s}{50\kappa_i + \kappa_s}$$

If $\kappa_s >> 50\kappa_i$ $\quad C \simeq \kappa_i$

If $50\kappa_i >> \kappa_s$ $\quad C \simeq \frac{\kappa_s}{50}$

If $\kappa_s = 50\kappa_i$ $\qquad C \simeq \frac{\kappa_i}{2}$

These proportionalities indicate that there is a desirable range such that $\kappa_i > \kappa_s > 50\kappa_i$

or more generally $\kappa_i > \kappa_s > \frac{W}{t_i}\kappa_i$

Of course this is a rather unsophisticated approach since W is a function of time and gate voltage. However, the purpose of this argument is to show that κ_i and κ_s cannot be arbitrarily chosen and that device performance can be deteriorated if the dielectric constants are drastically different.

6. Crystal Orientation

Surface states are created by the abrupt interruption of the periodic structure of the crystal lattice. This interruption ruptures the inter-molecular bonds of the valence electrons resulting in surface states that have a net positive charge associated with them. Generally, the more ruptured bonds the higher the surface state density. It then follows that the more bonds that are available for rupture the higher the surface state density. Crystal orientation should therefore be selected such that the cleaved axis provides the minimum number of ruptured valence bonds. For cubic structured crystals, such as silicon, the best orientation is <100> as demonstrated by Table I. A similar argument can be presented for certain small energy gap semiconductor compounds, such as InSb, which have

zinc blende structures. Generally <100> orientation provides the fewest number of bonds available for rupture so, all others effects being equal, it should be chosen as the preferable orientation.

PROPERTIES OF SILICON CRYSTAL PLANES

Orientation	Plane Area of Unit Cell (cm^2)	Atoms in Area	Available Bonds in Area	Atoms/cm^2	Available Bonds/cm^2
⟨111⟩	$\sqrt{3}a^2/2$	2	3	7.85×10^{14}	11.8×10^{14}
⟨110⟩	$\sqrt{2}a^2$	4	4	9.6×10^{14}	9.6×10^{14}
⟨100⟩	a^2	2	2	6.8×10^{14}	6.8×10^{14}

Table I

7. Chip Size

While it is possible to manufacture large silicon chips with high yield and low nonuniformities, these remarkable achievements are largely due to the very advanced state of silicon technology. The technology of narrow gap semiconductors needed for infrared applications is not nearly as advanced, and realizable chip sizes are correspondingly limited. Due to the longer wavelengths involved, infrared elements are larger and the element-per-chip density is reduced even further. These chip size constraints may be one of the reasons for utilization of thin film techniques for production of infrared arrays since good quality chips of large enough size may be grown using thin film techniques.

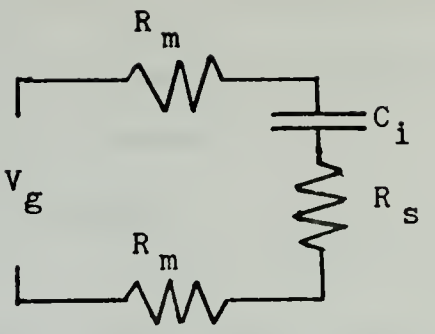
8. Array Size

The general trend in array sizes is toward large arrays containing a sufficient number of imaging elements to provide an image comparable to commercial television. The spatial non-uniformity problems associated with large area arrays are well documented [9], and indeed these problems are severe. Long linear surface channel CCD arrays are plagued by surface state noise problems [5]. Another important consideration in long linear arrays is the gate voltage pulse deterioration produced by the RC time constant of the array. This time constant affects the leading and trailing edge of the gate voltage pulse particularly near the end of a long array where the series resistance of the metal strip used for application of the gate voltage become significant. Also each added element provides additional parallel capacitance further increasing the time constant. For example consider the typical parameters of table II.

Array size: 1 X 500 elements
Cell area: 1 mil X 1 mil = 6.45 X 10^{-6} cm^2
Cell spacing: 3 microns
Insulator thickness: 1000 Å
Insulator dielectric constant: 40
Metal conductivity: 4 X 10^5 mhos/cm
Metal thickness: 1 micron
Metal width: 1 mil = 2.54 x 10^{-3} cm
Semiconductor thickness: 20 microns
Semiconductor resistivity: 3 ohm-cm

Table II

The RC time constant for the 500^{TH} element may be approximated by the equivalent circuit shown in figure 13.



TIME CONSTANT EQUIVALENT CIRCUIT

Figure 13

$$R = 2R_m + R_s$$

$$R_m = \left(\frac{2}{\sigma}\frac{\ell}{A}\right)_m = \frac{2}{4X10^{5}}\left(\frac{500(2.54X10^{-3}+3X10^{-4})}{(2.54X10^{-3})\ (1X10^{-4})}\right) = 28 \text{ ohms}$$

$$R_s = \left(\rho\ \frac{\ell}{A}\right)_s = 3\left(\frac{20X10^{-4}}{6.45X10^{-6}}\right) = 930 \text{ ohms}$$

$$C_i = \frac{\kappa\varepsilon_o A}{d} = \frac{(40)(8.854X10^{-14})(6.45X10^{-6})}{(0.1X10^{-4})} = 1.14X10^{-9}$$

then RC = 1 microsecond

and the gate voltage on the 500^{TH} element is

$$V_{500} = V_g e^{-RC/t}$$

so in order to get $V_{500}=0.9\ V_g$

$$e^{-RC/t} = 0.9$$

$$-RC/t = \ln 0.9 = -.1$$

then t = 10RC = 10 microseconds which limits the clock frequency to $f = \frac{1}{t} = 0.1$ MHZ

The importance of this calculation is that it shows that there is a trade off between array size, element capacitance, and clocking frequency.

9. Semiconductor Thickness

From the time constant and power dissipation constraints it is desirable to have thin semiconductors. However, thinning bulk materials to thickness of the order of tens of microns is difficult so thin film techniques appear desirable.

10. Insulator Thickness

Thin insulators provide higher insulator capacitance but fabrication of good quality, high resistivity insulators much less than 1000 angstroms is difficult. Therefore, the lower limit on insulator thickness will be set at 800 angstroms for the optimization calculation.

11. Temperature

In general it is desirable to have detectors operate in the range of normal ambient temperatures. Detector temperature has a profound effect on such semiconductor detector parameters as energy gap, intrinsic carrier concentration, resistivity, dark current, noise, etc. Cooling system costs usually vary immensly with operating temperature so, from that standpoint, the less cooling required the better. Some of the popular detector temperatures are $4^{o}K$ (liquid helium), $77^{o}K$ (liquid nitrogen), and $195^{o}K$ (dry ice).

B. OPTICAL PROPERTIES

The optical properties of an M-I-S infrared detector have a profound effect on its performance and must be considered as carefully as the electrical properties. Actually the optical and electrical performance cannot be handled separately because they are interactive.

1. Transmittance, Reflectance, and Absorptance

From the definitions of the above terms their sum must equal the normalized incident intensity. When a plane wave is normally incident upon an interface of two materials with differing indices of refraction, the transmittance

$$T = 1 - R$$

where R is the reflectance and may be approximated by

$$R \simeq \left(\frac{n_2 - n_1}{n_2 + n_1} \right)^2$$

where n_2 and n_1 are the indices of refraction of the two materials, if the effects of interference and extinction coefficient can be neglected. If several interfaces are encountered then the total reflectance is the product of the individual reflectances. The absorptance is

$$A = 1 - e^{-\alpha x}$$

where α is the coefficient of absorption and x is the distance into the material.

2. Quantum Efficiency

The total quantum efficiency of the device may be considered as two distinct but related problems. The first

is the degredation caused by reflection of radiation at the various device interfaces. The relationship between the quantum efficiency, η, and R is

$$\eta \propto (1 - R)$$

The second part of the quantum efficiency problem is related to the photon penetration depth into the detecting semiconductor, the associated absorption coefficient, and the electric field distribution within the semiconductor. Once a photon, with sufficient energy to create an electron-hole pair, enters the semiconductor the percentage of a absorption is

$$A = 1 - e^{-\alpha x}$$

where α is the absorption coefficient and x is the distance into the semiconductor. If the e-h pair generation occurs in a region where there exists and electric field (depletion region), then the electron and hole are rapidly separated and little recombination can take place. Essentially all minority carriers generated under such circumstances will be moved to and be stored in the inversion layer. If the depletion region is sufficiently deep such that $\alpha x = 3$ then

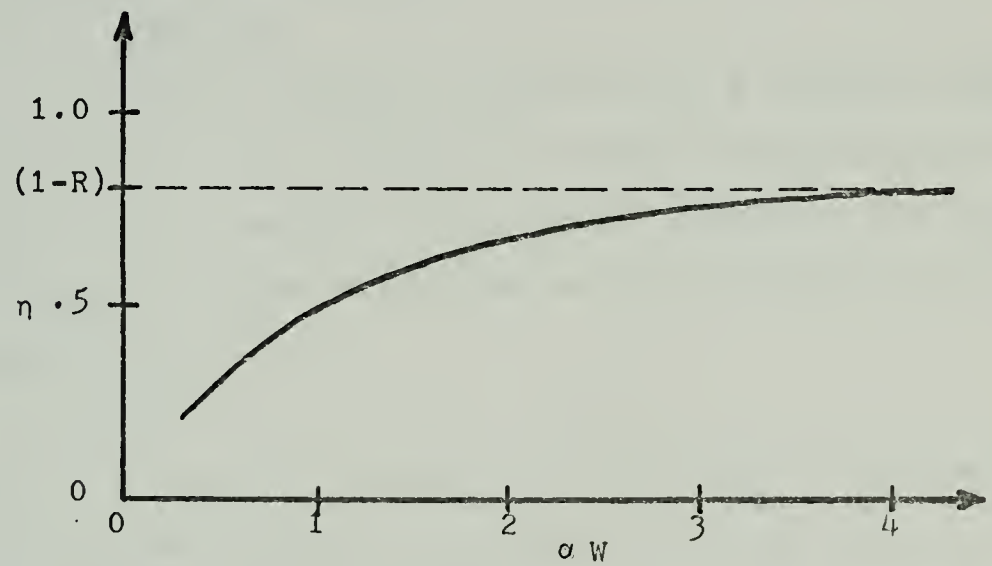
$$A = 1-e^{-3} = 95\%$$

This means that about 95% of the photons entering the semiconductor will be absorbed in the depletion region and will lead to stored charges in the inversion layer. The remaining 5% of the photons will be absorbed in the bulk and will

contribute to minority carrier storage in the inversion region if the photo-excited electrons can diffuse into the depletion region before recombination. The total quantum efficiency can be approximated by

$$\eta \simeq (1-R)(1-e^{-\alpha W})$$

The importance of the depletion width, W, in this formula cannot be overemphasized because as charge is stored in the inversion layer, W decreases.



QUANTUM EFFICIENCY DEPENDENCE ON DEPLETION WIDTH AND ABSORPTION COEFFICIENT

Figure 14

From Figure 14 it is obvious that in order to maintain a reasonable quantum efficiency, αW should be on the order of 3 or greater. This restriction reduces the storage capacity of the device as shown in Figure 12 and Appendix A.

3. Dynamic Range

Variations in photon flux density can present severe dynamic range problems. For high background photon flux density the charge integrating detector must integrate and

store all the background information as well as the signal information. Typically a $300^{o}K$ background, $0 < \lambda < 5$ microns, may generate some 10^{16} photons/sec-cm^2 while the signal may be on the order of 10^6 photons/sec-cm^2. Therefore the detector must have sufficient dynamic range to store a large number of background generated carriers as well as the signal.

C. ELECTRICAL PROPERITIES

1. Energy Gap

The basic detection mechanism in a depletion mode M-I-S device is the collection of photon generated minority carriers. The energy of the incident photon must be sufficient to produce a carrier transition across the energy gap of the semiconductor,

$$h\nu \geq Eg$$

where h is Planck's constant, ν is the photon frequency, and Eg is the semiconductor energy gap. Often this relationship is written as

$$\lambda_c = \frac{1.24}{Eg}$$

where λ_c is the critical (maximum) photon wavelength in microns which will produce a carrier transition across the energy gap, Eg (in electron volts). Many parameters such as pressure, magnetic fields, radiation, etc., can alter the energy gap of a given semiconductor. However, normally the most pronounced effect is that of temperature. Since temperature affects the energy gap of different semiconductors

in markedly different ways it is not prudent to list the mathematical relationship for all semiconductors. Specific formulas are used in the later optimization calculation. The energy gaps of ternary compounds such as $Pb_{1-x}Sn_xTe$, $Pb_{1-x}Sn_xSe$, and $Hg_{1-x}Cd_xTe$ are a function of the value of x in the chemical expressions and can be made to cover a large part of the infrared spectrum. This is a great advantage since an advanced technology on any one of these would be widely applicable throughout the infrared and might permit operation at higher temperatures if the thermal noise problems could be minimized. The possible applications of a room temperature silicon/narrow-gap semiconductor device are indeed promising.

2. Doping Level

Generally for InSb, doping levels below 10^{13} per cm^3 are not achievable without adding compensation impurities which produce undesirable effects on other crystal properties. Therefore, this study will not consider doping levels below 10^{13} per cm^3. On the other extreme, doping levels above 10^{18} per cm^3 are not good quality semiconductor crystals and hence they will not be considered. The device doping level affects the depletion width, surface potential, storage capacity, storage time, dark current, and quantum efficiency. Refer to those sections and the system optimization calculation for further discussion.

3. Carrier Lifetime

Carrier lifetimes play an important role in all design processes involving semiconductor materials. In any case carrier lifetimes must be longer than the time required to perform any operation using them. For depletion mode M-I-S design the generation-recombination lifetime and minority carrier lifetime are of importance. The lifetime of minority carriers stored in the inversion layer is determined by dark current and surface state recombination and trapping. However, these effects are minimal and very long inversion layer minority carrier lifetimes are typical [17] [24] [27]. Simply, if the lifetime of stored minority carriers was not long, the inversion layer could not form and charge storage would be impossible. The generation of minority carriers in the presence of the electric field of the depletion region produces the charge which will be stored in the inversion layer. It is necessary that the photon generated minority carriers have sufficient lifetime to reach the inversion layer before they can recombine with electrons. This means that the generation-recombination lifetime, τ_{GR}, must be greater than the ratio of depletion width, W, to average drift velocity, $\bar{v}$.

$$\tau_{GR} >> \frac{W}{\bar{v}} = \frac{W}{\mu\varepsilon} = \frac{W}{\mu\frac{\Psi_s}{W}} = \frac{W^2}{\mu\Psi_s}$$

Typically W is a few microns, Ψ_s is a few volts and μ is 10^4 or 10^5 cm^2/v-sec.

$$\tau_{GR} >> \frac{(5X10^{-4})^2}{(10^4)(10)} = 25X10^{-11}\text{sec}$$

This inequality is easily satisfied and therefore does not constrain M-I-S design appreciably. However, dark current generated within the depletion region can have a severe effect on storage time and constrains τ_{GR} appreciably [1] [22]. The dark current minority carrier generation rate must be substantially less than the photon minority carrier generation rate. For a photon flux density of 10^{16} photons/cm^2-sec incident on a typical InSb device the constraint is

$$\tau_{GR} >> \frac{n_i \sqrt{\frac{\varepsilon_s q \psi_s}{2 N_D}}}{q Q_B}$$

$$\text{or} \quad \tau_{GR} >> \frac{10^{10} \sqrt{\frac{(160X10^{-14})(1.6X10^{-19})(10)}{2X10^{14}}}}{(1.6X10^{-19})(10^{16})} = 10^{-9}\text{sec}.$$

This indicates that τ_{GR} on the order of 10^{-7} or 10^{-6} seconds are desirable to satisfy the inequality [7] [12] [18]. On the other hand, the charge injection readout scheme relies on minority carrier recombination in the bulk semiconductor and the time required for this process is τ_{GR}. Hence, the speed of the elementary CID is limited to $1/\tau_{GR}$ or about a few megahertz. Some techniques to relax this limitation are discussed in the Operational Improvement Techniques section of this report. Since part of the dark current results from minority carrier thermal generation within a diffusion

length of the depletion region, this generation rate must also be much smaller than the depletion region photon minority carrier generation rate or

$$\tau_m >> \frac{\left(\frac{qn_i^2}{N_D}\sqrt{\frac{\mu_m kT}{q}}\right)^2}{q Q_B}$$

or typically

$$\tau_m >> \frac{\left(\frac{(1.6X10^{-19})(10^{10})^2}{10^{14}}\sqrt{\frac{(10^4)(1.38X10^{-23})(77)}{1.6X10^{-19}}}\right)^2}{(1.6X10^{-19})(10^{16})}$$

or $\tau_m >> 10^{-18}$ seconds

This is not a particularly demanding requirement for low detector temperature, high photon flux density applications. Another constraint on minority carrier lifetime in CCD applications is that the carriers must be able to survive the well-to-well transfer process. This means that τ_m must be much longer than the transfer time, τ_{tr}. In the well-to-well transfer process three mechanisms cause the charge to move; drift, repulsion, and diffusion [5]. The time required for the drift process may be approximated by

$$\frac{\ell}{\bar{v}} = \frac{\ell^2}{\mu(\Psi_2-\Psi_1)}$$

where ℓ is the intercell distance and $(\Psi_2-\Psi_1)$ is the surface potential between adjacent wells. Typically

$$\frac{\ell^2}{\mu(\Psi_2-\Psi_1)} = \frac{(20 \times 10^{-4})^2}{(10^4)(10)} = 4 \times 10^{-11} \text{ sec.}$$

and since

$$\tau_m >> 4 \times 10^{-11} \text{seconds}$$

the transfer is not normally limited by the drift mechanism. Mutual repulsion forces between the charged carriers will cause some of them to move into the electric field region where they will be rapidly transferred to the adjacent potential well. This is a statistical phenomena whose effect is not constant for all the remaining charges but the effect on some of the charges may be approximated by

$$\frac{\ell}{\bar{v}} \simeq \frac{\ell}{\sqrt{\frac{q^2}{4\pi \varepsilon_s r \cdot m}}}$$

and typically

$$\frac{\ell}{\bar{v}} = \frac{20 \times 10^{-6}}{\sqrt{\frac{1.6 \times 10^{-19}}{(4)(\pi)(18)(8.854 \times 10^{-12})(6 \times 10^{-10})(9.1 \times 10^{-31})}}}$$

$$\simeq 10^{-10} \text{ seconds}$$

and since $\tau_m >> 10^{-10}$ seconds

the transfer time is not normally limited by mutual repulsion. The remaining charges can be moved only by a diffusion process and this transfer time is approximated by $\ell^2/4D$ where D is the diffusion constant [12]. Then typically

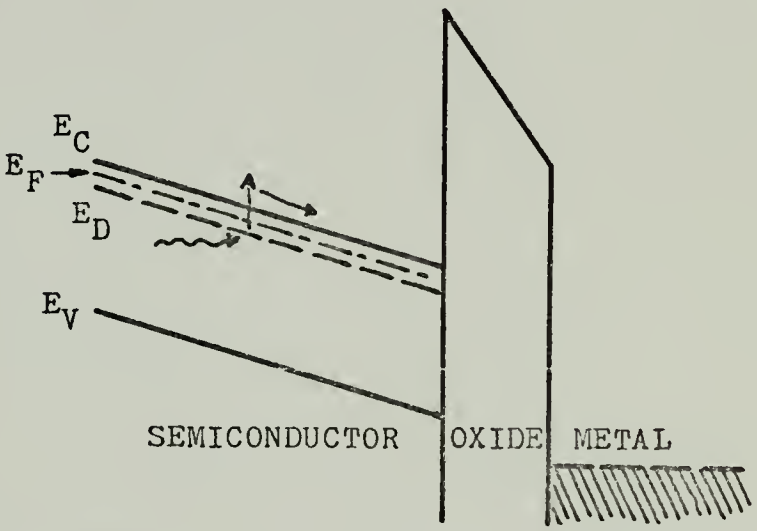
$$\frac{\ell^2}{4D} = \frac{(20X10^{-4})^2}{(4)(100)} = 10^{-8} \text{ seconds}$$

and τ_m is not normally much greater than 10^{-8} seconds. Therefore the process of nearly complete charge transfer is limited by diffusion. Thus, the shorter τ_m is, the shorter τ_{tr} must be and reduction of τ_{tr} can be accomplished by making ℓ smaller, or increasing μ and the surface potential between wells. Fabrication techniques and cross-talk problems limit how close together the cells can be and power dissipation limits the potential values. Then increasing μ in the transfer region seems to be a way to improve performance and has been done [5]. The section on Operational Improvement techniques briefly considers this and other ideas.

4. Carrier Type

If the surface states have a positive charge associated with them (such as found in silicon and InSb), it is desirable to have electrons stored in the inversion layer and keep the surface states filled. Then surface state influence on device operation can be reduced [16]. Since semiconductor work functions (electron affinities) are generally larger than metal work functions the flat band voltage is negative. This can be an asset for low gate voltage (TTL compatible without level shifters) operations since a p-type device will be slightly depleted or inverted at zero applied bias. Therefore a larger storage capacity can be realized for the same gate voltage. Generally, electron mobility is higher than hole mobility and since the minority carriers represent

the signal in a depletion mode device, speed should be better in p-type M-I-S devices. This speed advantage coupled with the great attraction of using extrinsic silicon for long wavelength infrared charge transport imaging has created interest in n-type accumulation mode devices [25]. Figure 15 shows the energy band diagram of an accumulation mode M-I-S device.



ACCUMULATION MODE ENERGY BAND DIAGRAM

Figure 15

Some other advantages of using electrons to represent the stored signal will be demonstrated in the system calculation.

5. Gate Voltage

The general constraints on gate voltage are device power dissipation, ease of generating clock pulses of the required amplitude, and semiconductor breakdown. However, if the clock generation is to be accomplished using transistor-transistor-logic (TTL), then it is desirable

that the detectors be compatible without the need for level shifters. Power supplies for these circuits normally generate voltages in the range of 0-5 volts. If pulse amplitudes up to 15 or 20 volts are needed, more complicated TTL to MOS level shifters will have to be used.

IV. OPERATIONAL IMPROVEMENT TECHNIQUES

Several techniques have been proposed and some have been demonstrated which improve the detector or system performance. These techniques may be classified as M-I-S, CCD, and CID techniques. The first of these is a single detector device while the latter two are array and system applicable. Subsequent to a discussion of these techniques a CID structure is proposed incorporating many of these techniques.

A. M-I-S DETECTOR IMPROVEMENTS

The two most outstanding features of an M-I-S infrared detector are its ability to efficiently utilize the incoming photons and its ability to store the photon generated carriers. Consequently, improvement of quantum efficiency and storage capability are desirable and some of those techniques are discussed below.

1. Transparent Gates

When the incident photons are arriving from the metal side of the device, it is desirable that the gates be as transparent as possible to reduce absorption losses. Some transparent gates such as poly-silicon have been developed [19] which absorb less radiation than would a metal gate. Normally these gates have lower conductivity than metal gates and therefore pose potential power dissipation and gate voltage pulse deterioration problems particularly in large array applications.

2. Thin-Film Semiconductors

The principal optical efficiency improvement gained by using thin-film semiconductors is that the device may be back-side illuminated. Not only does this technique permit the use of high quality opaque metal gates, it also provides a structure conducive to other optical improvements such as anti-reflection layers and increased sensitive area size. Group IV-VI binary and ternary compound thin-film fabrication has been demonstrated [21] [29] and seems promising since the larger dielectric constants also promote better storage capability. Of course, their higher capacitances will deteriorate the wave shape of the driving clock pulses, especially in a large array.

3. Back-Illumination

The principal advantages of back-illumination are the lack of a need for transparent gates and better utilization of the device sensitive area. Optical efficiency can be improved in back-illuminated devices by using anti-reflection layers. Absorption of incoming photons in the bulk semiconductor outside the depletion region severely restricts the use of material such as InSb bulk crystals in a back-illuminated device because they cannot be thinned down to tens of microns thick in production process. Thin-film devices, however, provide the ability to deplete the entire semiconductor eliminating bulk absorption and therefore improving quantum efficiency. The effects of complete depletion of the semiconductor, at the semiconductor back

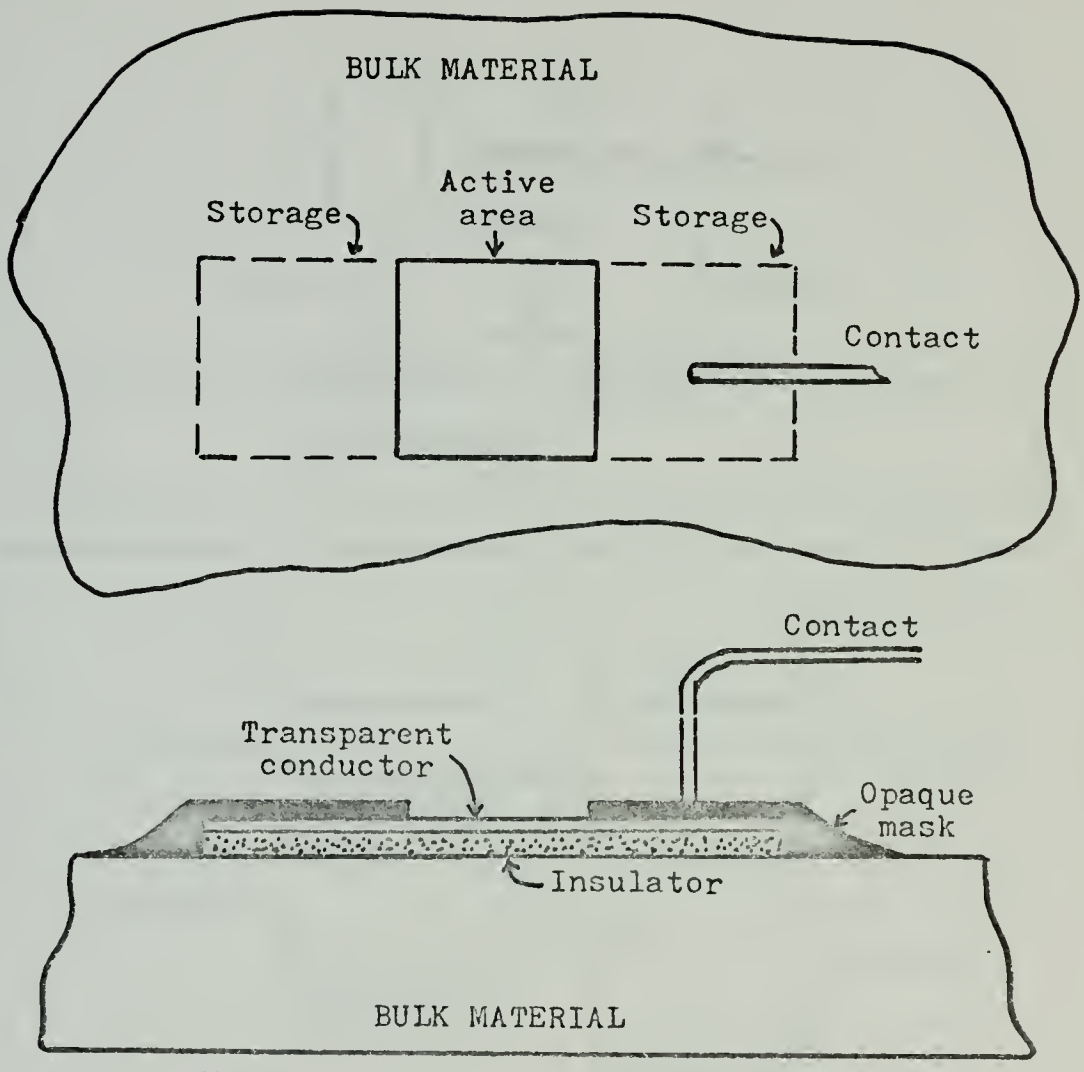
interface, have not been much studied yet. Solution of the boundary condition problem at this interface is desirable to determine these effects on the device performance produced by complete depletion of the semiconductor.

4. Anti-Reflection Layers

The use of anti-reflection layers to reduce reflection losses at the interface of two materials with differing indices of refraction is well documented [14]. Such layers may also be used particularly in back-illuminated M-I-S structures. For example, the barium fluoride substrate on which IV-VI semiconductor material has been grown displays good anti-reflection layer properties [29]. Of course, the anti-reflection layer's coefficient of absorption must be very low for this technique to be useful.

5. Dynamic Range Extension

The fundamental dynamic range limitation in charge storage devices is their capacity to store charge. This is particularly important in infrared applications where the high backgound temperatures require detectors with larger dynamic ranges. Increasing the storage area while maintaining the optically sensitive area will improve dynamic range [1]. Such a scheme is shown in Figure 16. However, this arrangement has some drawbacks. If front-illumination is used a transparent conductor is required, and the technique is limited to linear or bi-linear arrays if resolution is to be conserved.

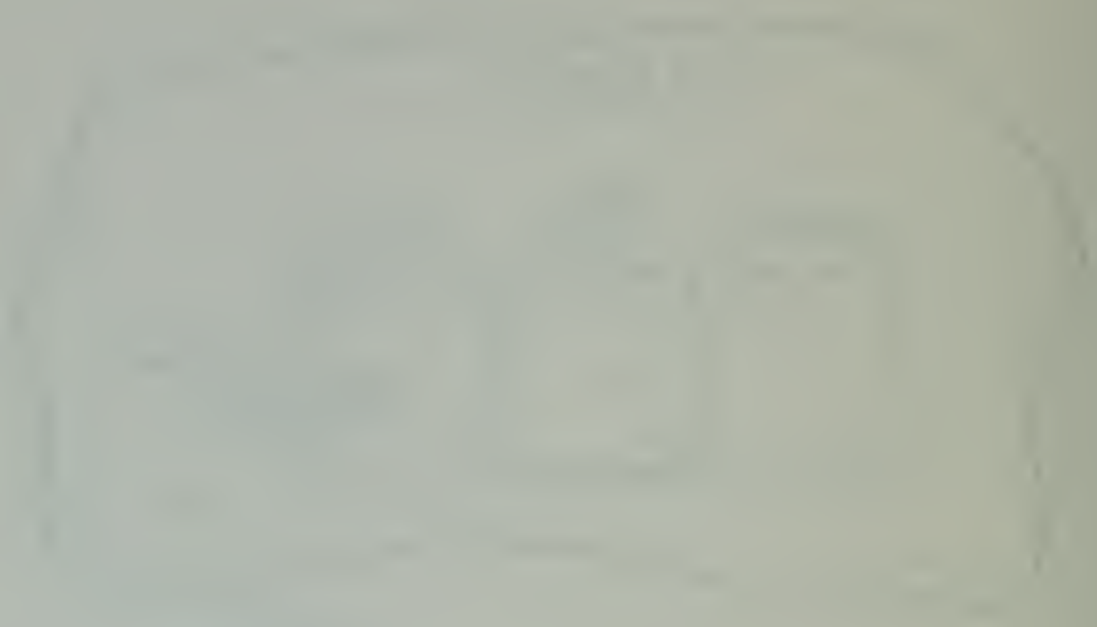


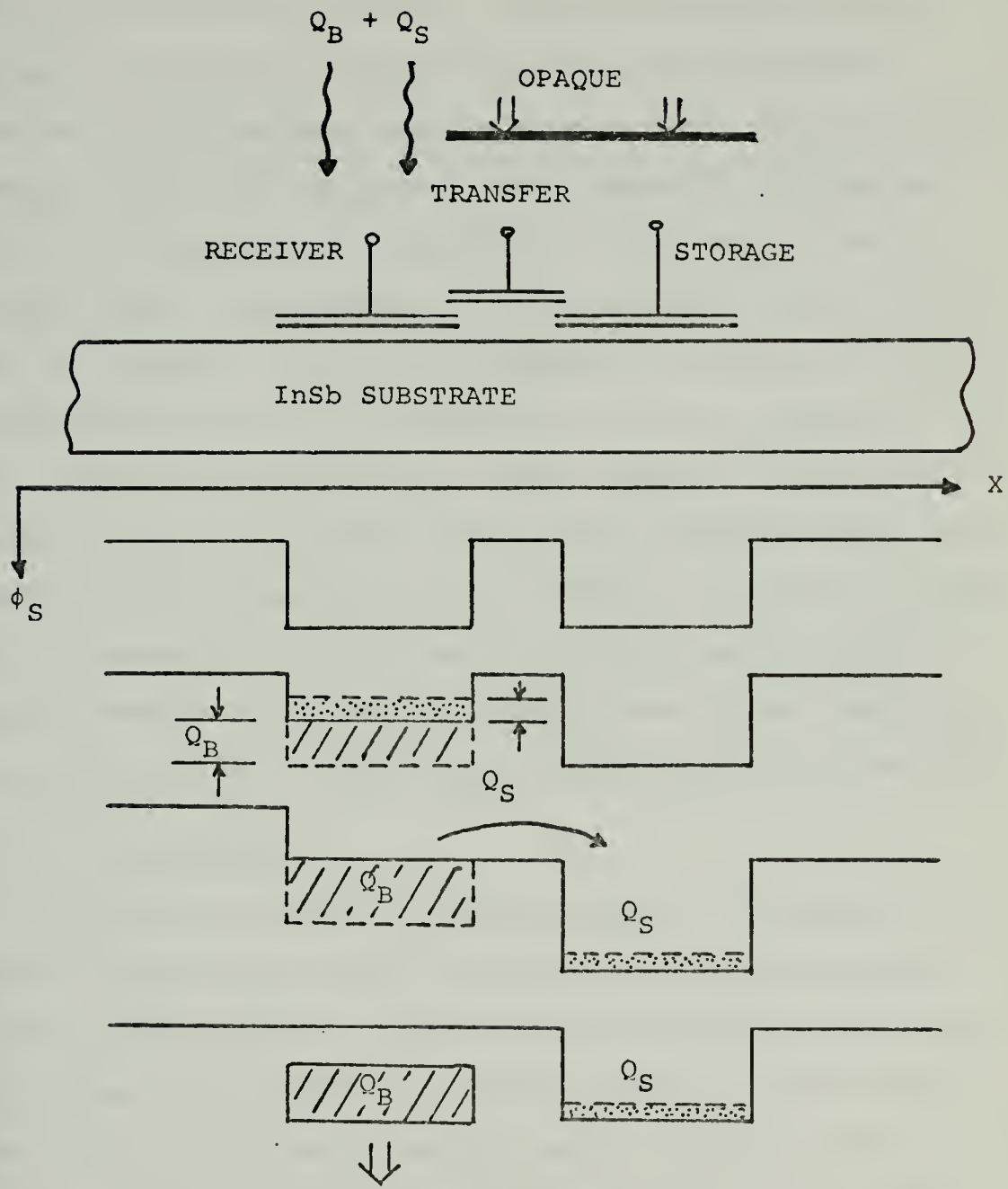
DYNAMIC RANGE EXTENSION STRUCTURE

Figure 16

6. Background Suppression

In high background infrared M-I-S imaging the large background signal must be stored as well as the signal. The large d.c. level created by the background contains no signal information and should be excluded. Figure 17 shows the basic operation of a proposed technique to suppress the effects of the high background level [1].





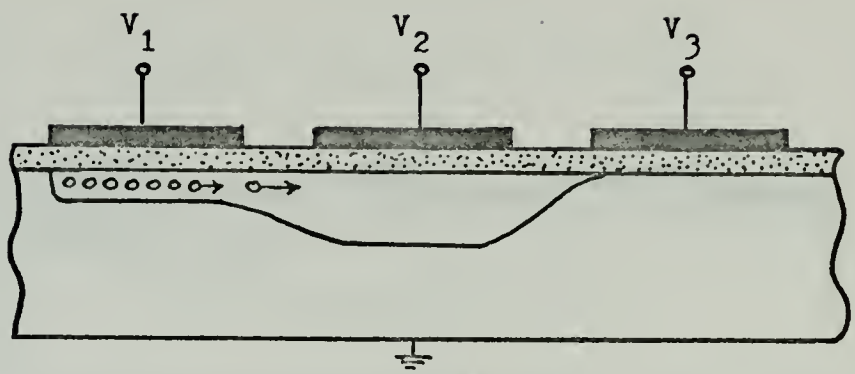
BACKGROUND SUPPRESSION STRUCTURE AND OPERATION

Figure 17

The receiver gate is optically sensitive in the generation of photon produced carriers and stores them during the receiver exposure period. Then the transfer gate is pulsed to transfer a controlled portion of the stored carriers by CCD action into the storage well. The remaining charge in the receiver gate is then removed by CID action and the receiver gate is depleted to start the exposure process again. After several cycles and before the storage well is saturated, the charge stored in the storage well may be read out by CCD or CID action. The net effect is that longer integration time of the unexposed storage well may be utilized to improve the signal-to-noise ratio of the structure. The drawbacks to this scheme are again the need for a transparent receiver gate electrode and the reduced spatial resolution in staring arrays because the area taken by the storage and transfer gates is not optically sensitive.

B. CCD IMPROVEMENTS

The primary areas of CCD improvements are increased speed of operation, better transfer efficiency and lower transfer noise which are all related to the charge transfer mechanisms. The movement of charge stored in an inversion layer into an adjacent potential well is accomplished by diffusion and drift [5]. The charges stored in the inversion region near the right hand side of gate 1 are influenced by the electric field produced by the difference in surface potential between gates 1 and 2.



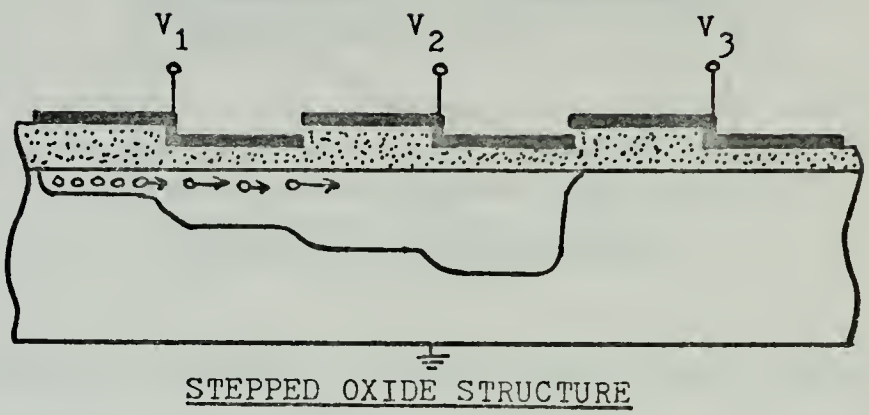
CCD CHARGE TRANSFER

Figure 18

The average carrier velocity in this region is $\bar{v}=\mu$ and is quite fast compared to the diffusion velocity of the carriers under most of the area of gate 1. Mutual repulsion will cause the stored charge movement but the last few percent diffuse at a much reduced speed. Thus the transfer speed is limited by the diffusion mechanism if nearly complete transfer is desired. Some of the more obvious improvements such as higher gate voltages and smaller gates have adverse effects on power supply requirements and storage capacity respectively. Some of the not-so-obvious improvements are discussed below.

1. Stepped Oxide

The concept of stepped oxides provides a variation in the surface potential under a single gate as shown in Figure 19.



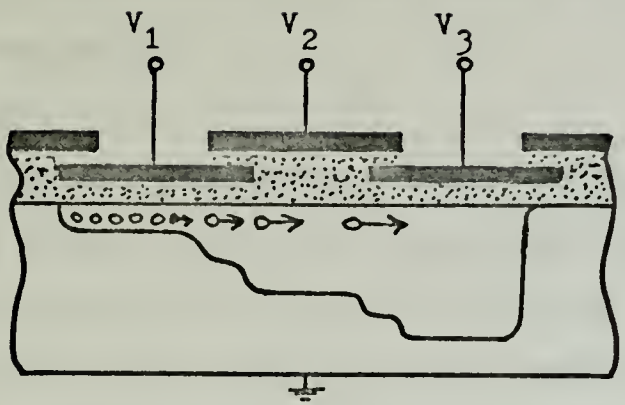
STEPPED OXIDE STRUCTURE

Figure 19

The transfer process is speeded up since more of the stored carriers are under the influence of an electric field and move with drift velocity which is generally higher than diffusion velocity. The step need not be abrupt and if graded continuously beneath the metal gate, speed would be enhanced since nearly all stored carriers would be placed in an electric field. The major drawback to this is that such devices are more difficult to manufacture. Another less serious limitation, worth mentioning in passing, is that charges can be transferred only in one direction.

2. Overlapping Gates

The concept of overlapping gates is similar in orgin to stepped oxide. Although the main purpose is to eliminate the gap problem between gates, the transfer could be helped because carriers now move under an electric field between gates. Figure 20 shows the general structure.

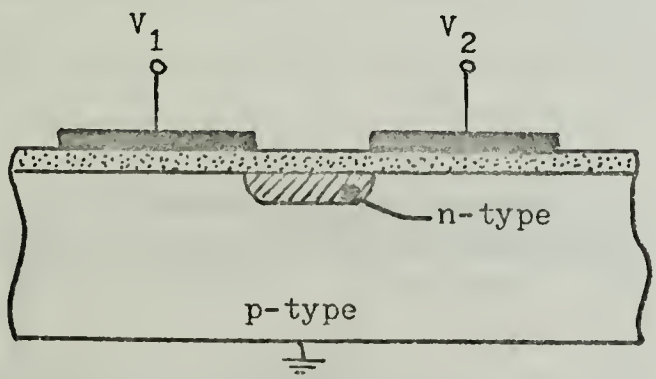


OVERLAPPING GATE STRUCTURE
Figure 20

Device operation is similar to the stepped oxide operation.

3. Transfer Channel Doping

Thus far the improvement techniques have dealt with speed improvements resulting from increasing the effectiveness of the electric field without taking advantage of the possibility of increasing carrier mobility. Generally, electron mobility is higher than hole mobility so electrons will diffuse faster than holes. This indicates that p-type (n channel) material should be used to improve speed. Transfer channel doping may also be used to improve speed by creating a high mobility region between the gates as shown in Figure 21.



DOPED TRANSFER CHANNEL STRUCTURE
Figure 21

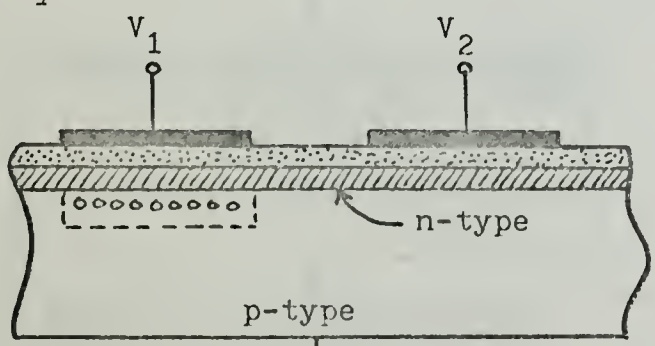
The main disadvantage of this scheme is the increased manufacturing complexity.

4. "FAT Zero"

Another serious problem is created by carrier exchange with the surface states, which will cause poor transfer efficiency and surface state noise. The concept of using "FAT Zero" to reduce these effects is that sufficient carriers are introduced into the inversion region filling the interface surface states and thus minimizing signal carriers being trapped by the surface states. No special structure is required but care must be taken to insure that the FAT zero injection itself does not contribute appreciably to device noise.

5. Buried Channel

The buried channel configuration arose from the same premises as FAT zero, that is, to reduce the detrimental effects of surface states. A buried channel CCD essentially moves the charge storage and transfer regions away from the insulator-semiconductor interface by creating a "semiconductor-semiconductor" interface. This is accomplished by creating a p-n junction away from the insulator as shown in Figure 22.



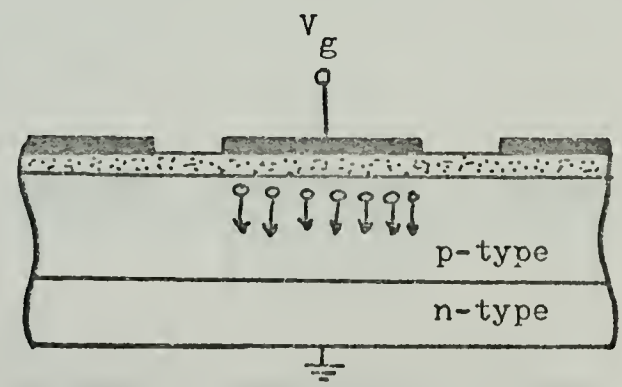
BURIED CHANNEL STRUCTURE
Figure 22

This configuration not only reduces the detrimental effects of surface states but increases transfer speed as well. The buried channel CCD has proven to be a very viable structure. The major drawback is more complexity of manufacturing but making this p-n junction layer by ion implantation is being steadily developed and the problems should be under control in the near future.

C. CID IMPROVEMENTS

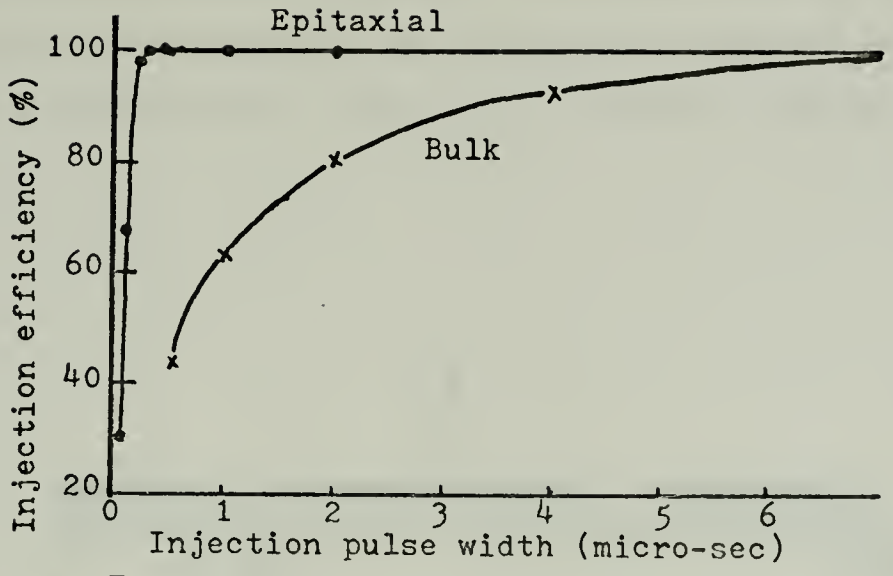
1. Epitaxial Layer

Charge injected into the bulk during readout of a CID sensing site must recombine or diffuse away to avoid interference with subsequent readouts. For long generation-recombination lifetime material, this time is on the order of microseconds and will limit the readout clocking frequency. A structure which improves the speed of operation may be achieved by means of a back epitaxial layer which forms a diode [3]. The structure is shown in Figure 23 while Figure 24 illustrates the injection efficiency improvement.



EPITAXIAL LAYER STRUCTURE

Figure 23



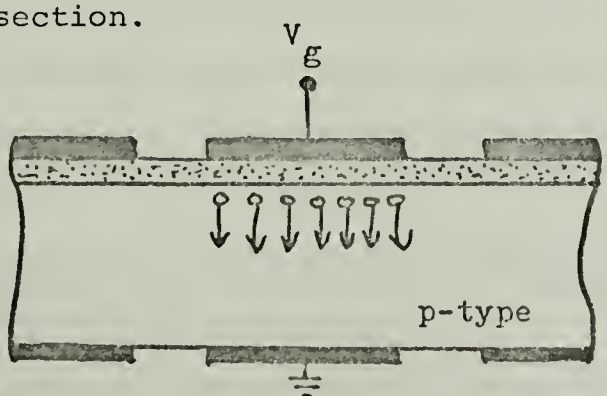
EPITAXIAL LAYER INJECTION EFFICIENCY

Figure 24

Reverse biasing the back epitaxial layer during injection improves the speed even more and can virtually eliminate the injection time as a limit to readout speed for the CID imager.

2. Schottky Barrier

The structure shown in Figure 25 may also be used to increase the speed of a CID. Here the Schottky barrier performs essentially the same function as the epitaxial layer of the previous section.



SCHOTTKY BARRIER STRUCTURE

Figure 25

D. PROPOSED NEW STRUCTURE

From the previous discussions a new structure was devised which incorporates many of the improvement features into a single CID structure. Figure 26 illustrates the structure.

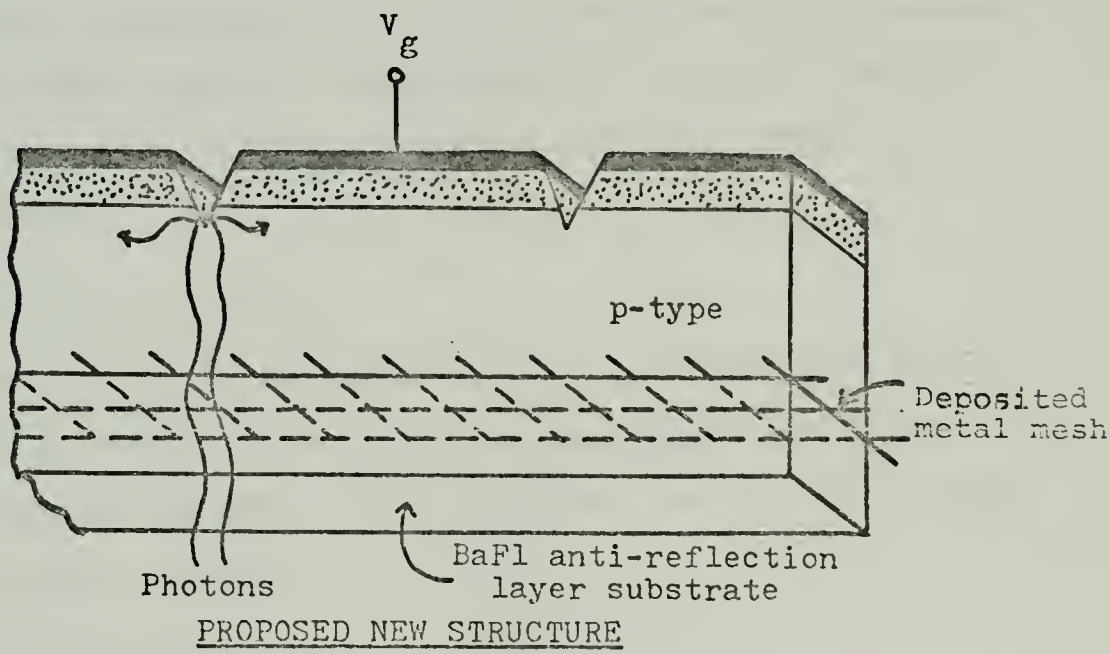


Figure 26

Briefly stated, the advantages of this structure are:

(1) Thin film semiconductor permits back-illumination.

(2) Back-illumination permits the use of substrate as anti-reflection layer and opaque metal gates on the insulator.

(3) If the semiconductor layer is etched into different cells internal reflection at cell boundaries could improve collection efficiency.

(4) Metal mesh deposited on the substrate provides Schottky barrier junction for speed improvement.

(5) Fabrication is monolithic.

V. OPTIMAL DEVICE DESIGN EXAMPLE

To optimize the design parameters of an infrared charge transport device detector some logical sequence of analysis must be performed. This section described the optimization method which determines the optimized set of device parameters for a particular system. The procedure is general enough to be applicable to a variety of systems with only minor modifications.

A. STATEMENT OF THE GOAL

The first step in any optimization is to establish the goal of the design process, that is, what capabilities the final system should have. For this study the following system objectives were selected.

Spectral range:	3-5.5 microns
Background temperature:	290° Kelvin
Frame time:	1/30 second
Spatial resolution:	comparable to present television standards
Voltage requirements:	15 volts or less
Time constraint:	system desired as soon as possible
Weight/Size:	system will be housed in typical Navy aircraft

B. OPTIMIZATION USING InSb (FRONT-ILLUMINATION)

1. Basic Material Selection

a. Semiconductor

Based on the spectral range and state-of-the-art narrow-gap semiconductor technology, Indium Antimonide (InSb)

may be selected as the semiconductor material. Table III lists the characteristics of InSb at 77°K, which is the desirable operating temperature.

E_g = 0.218 ev

χ = 4.57 volts

n_i = 2.7×10^{9} cm^{-3}

κ_s = 18.0

μ_e = 5.0×10^{5} cm^2/volt-sec

μ_n = 1.0×10^{4} cm^2/volt-sec

τ_{e_p} = 2×10^{-10} sec

τ_{h_n} = 5×10^{-8} sec

τ_{GR} = 1×10^{-7} sec

ρ_p = .06 - 6 ohm cm

ρ_n = 10^{-3} - 10^{-1} ohm cm

α = 4000 cm^{-1}

ℓ = 6.50×10^{-6} per °C

n = 4

Table III

To reduce anticipated surface state density, <100> crystal orientation was selected. Since it has not been demonstrated that InSb can be thinned sufficiently down to ten microns or so for high yield production, front side illumination will be used. Transparent poly-silicon

gates will enhance the optical sensitivity. The thickness of the InSb is not too crucial but it is desirable to have as small a thickness as possible for faster speed and less power dissipation.

b. Insulator

The selection of InSb as semiconductor will influence the choice of insulator material because the insulator thermal expansion coefficient, dielectric strength, and dielectric constant should be in the ranges previously discussed. Insulators such as SiO_2, Al_2O_3, anodized native oxide, Ta_2O_5, and TiO_x have been considered [16] [24] [28]. One or a combination of these insulator materials will be used.

c. Metal

The selection of the gate metal principally depends on the feasibility of a good bond with the insulator, and whether or not transparent gates are desired. Although, the metal semiconductor work functions also enter into the consideration somewhat. For this calculation, poly-silicon gates will be used since back side illumination is not considered practical due to the available semiconductor thickness.

2. Computer Calculation Results

The selection of the remaining parameters will be optimized with the assistance of computer programs. The program devised for this calculation is given in Appendix C.

INITIAL DEPLETION WIDTH (microns)
50
40
30
20
10
0
100
200
300
400
500
600
700
K_i/t_i (per micron)
N_A=1X10^{13}
N_A=3X10^{13}
N_A=5X10^{13}
N_A=7X10^{13}
N_A=1X10^{14}
N_A=3X10^{14}
Al_2O_3 880Å
Ta_2O_5 TiO_2 7500Å
Al_2O_3 440Å
Ta_2O_5 2000Å
TiO_2 3250Å
Al_2O_3 293Å
Ta_2O_5 1333Å
TiO_2 2500Å
Al_2O_3 220Å
Ta_2O_5 1000Å
TiO_2 1875Å
Al_2O_3 176Å
Ta_2O_5 800Å
TiO_2 1500Å
Al_2O_3 142Å
Ta_2O_5 667Å
TiO_2 1250Å
Al_2O_3 126Å
Ta_2O_5 571Å
TiO_2 1071Å

Figure 27

INITIAL SURFACE POTENTIAL (Normalized to V_{∞})
1.0
.97
.94
.91
.88
.85
100
200
300
400
500
600
700
κ_i/t_i (per micron)
$N_A=1X10^{13}$
$N_A=3X10^{13}$
$N_A=5X10^{13}$
$N_A=7X10^{13}$
$N_A=1X10^{14}$
$N_A=3X10^{14}$
880Å Al_2O_3 4000Å Ta_2O_5 7500Å TiO_2
440Å Al_2O_3 2000Å Ta_2O_5 3750Å TiO_2
293Å Al_2O_3 1333Å Ta_2O_5 2500Å TiO_2
220Å Al_2O_3 1000Å Ta_2O_5 1875Å TiO_2
176Å Al_2O_3 800Å Ta_2O_5 1500Å TiO_2
147Å Al_2O_3 667Å Ta_2O_5 1250Å TiO_2
126Å Al_2O_3 571Å Ta_2O_5 1071Å TiO_2

Figure 28

NUMBER OF CHARGES STORED (X10^{13} ,per square cm)
1
2
3
4
5
100
200
300
400
500
600
700
κ_i/t_i (per micron)
SMAX=$C_i V_g/q$
N_A=7X10^{13}
N_A=1X10^{14}
N_A=1X10^{13}
N_A=3X10^{13}
N_A=5X10^{13}
N_A=3X10^{14}
880A Al_2O_3
4000A Ta_2O_5
7500A TiO_2
440A Al_2O_3
2000A Ta_2O_5
3250A TiO_2
293A Al_2O_3
1333A Ta_2O_5
2500A TiO_2
220A Al_2O_3
1000A Ta_2O_5
1875A TiO_2
1500A TiO_2
800A Ta_2O_5
126A Al_2O_3
1250A TiO_2
662A Ta_2O_5
147A Al_2O_3
1071A TiO_2
571A Ta_2O_5
126A Al_2O_3

Figure 29

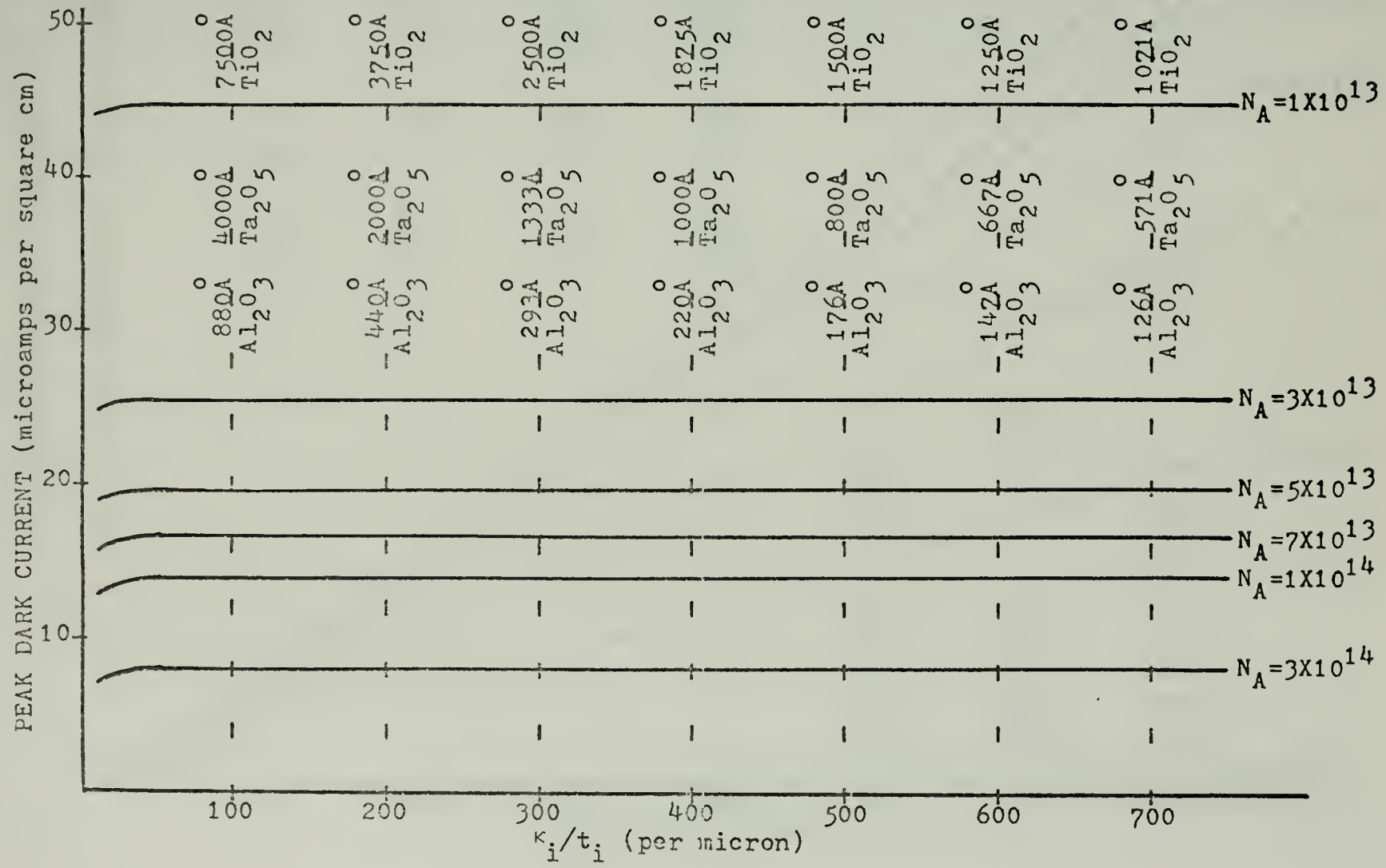

PEAK DARK CURRENT (microamps per square cm)
50
40
30
20
10
100
200
300
400
500
600
700
K_i/t_i (per micron)
7500A TiO_2
3750A TiO_2
2500A TiO_2
1875A TiO_2
1500A TiO_2
1250A TiO_2
1071A TiO_2
4000A Ta_2O_5
2000A Ta_2O_5
1333A Ta_2O_5
1000A Ta_2O_5
800A Ta_2O_5
667A Ta_2O_5
571A Ta_2O_5
88A Al_2O_3
44A Al_2O_3
29.3A Al_2O_3
22A Al_2O_3
17.6A Al_2O_3
14.2A Al_2O_3
12.6A Al_2O_3
$N_A=1X10^{13}$
$N_A=3X10^{13}$
$N_A=5X10^{13}$
$N_A=7X10^{13}$
$N_A=1X10^{14}$
$N_A=3X10^{14}$

Figure 30

DARK INTEGRATION TIME (seconds)
0.5
0.4
0.3
0.2
0.1
0
100
200
300
400
500
600
700
K_i/t_i (per micron)
$N_A=1X10^{14}$
$N_A=3X10^{14}$
$N_A=7X10^{13}$
$N_A=5X10^{13}$
$N_A=3X10^{13}$
$N_A=1X10^{13}$
Al_2O_3 880Å Ta_2O_5 400Å TiO_2 250Å
Al_2O_3 440Å Ta_2O_5 200Å TiO_2 375Å
Al_2O_3 293Å Ta_2O_5 1333Å TiO_2 250Å
Al_2O_3 220Å Ta_2O_5 1000Å TiO_2 1875Å
Al_2O_3 126Å Ta_2O_5 800Å TiO_2 1500Å
Al_2O_3 147Å Ta_2O_5 667Å TiO_2 1250Å
Al_2O_3 126Å Ta_2O_5 571Å TiO_2 1071Å

Figure 31

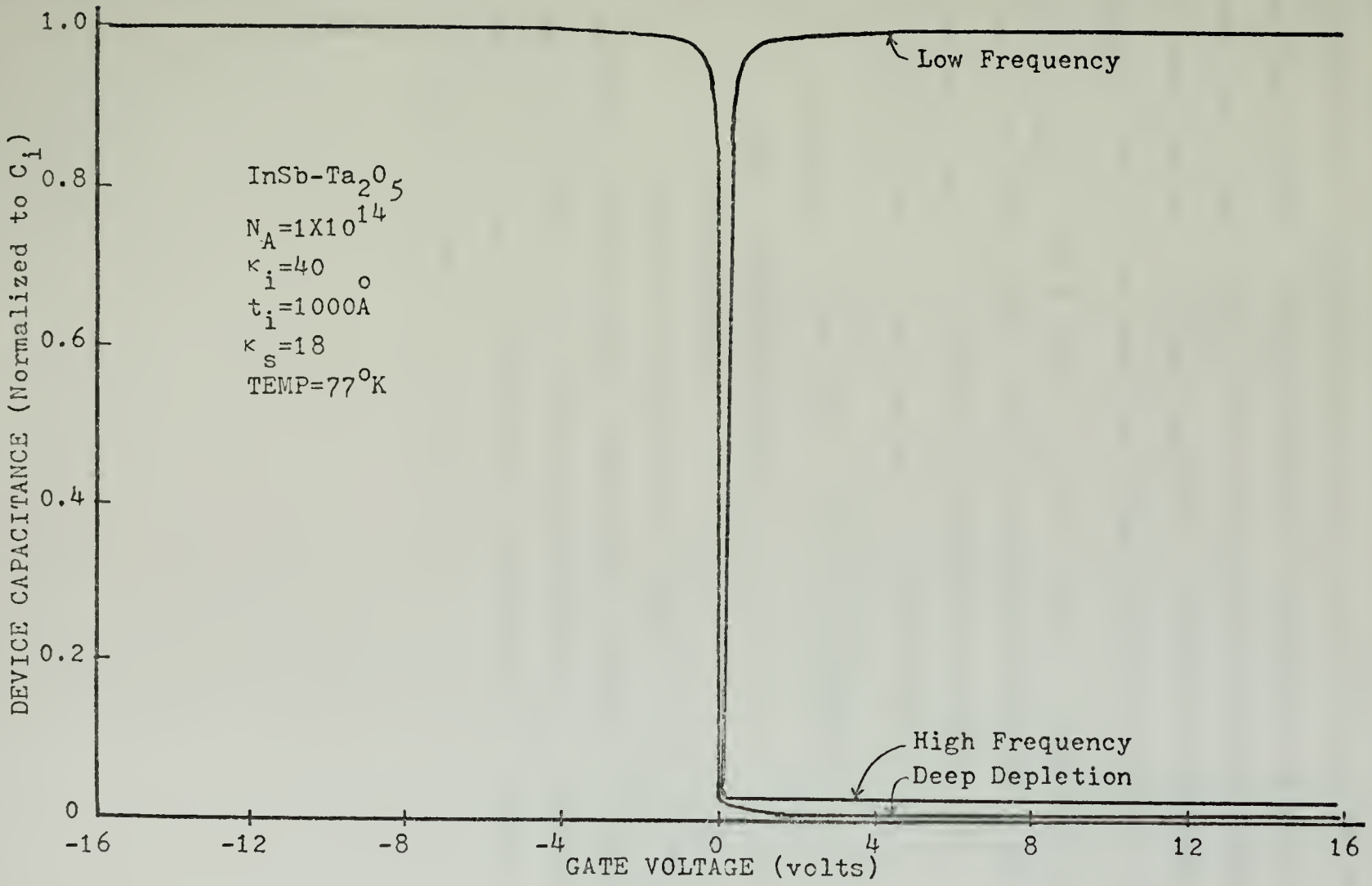

1.0
0.8
0.6
0.4
0.2
0
DEVICE CAPACITANCE (Normalized to C_i)
InSb-Ta_2O_5
N_A=1X10^{14}
κ_i=40
t_i=1000A
κ_s=18
TEMP=77°K
Low Frequency
High Frequency
Deep Depletion
-16
-12
-8
-4
0
4
8
12
16
GATE VOLTAGE (volts)

Figure 32

The resulting plots are shown in Figures 27 through 31. For completeness, Figure 32 shows the C-V curve for one of the optimum devices. From the computer calculation it can be seen that lower doping levels and higher insulator capacitance provide the best storage capability. Within the material constraints, a good combination was selected as $N_D = 1 \times 10^{14}$ cm^{-3}, $t_{ins} = 1000$ Å, and $K_{ins} = 40$ (Ta_2O_5). This provides for 2.7×10^{13} charges stored per square centimeter. The depletion width is sufficient to preserve good quantum efficiency and the dark current is sufficiently low.

C. OPTIMIZATION USING PbTe (FRONT-ILLUMINATION)

1. Basic Material Selection

a. Semiconductor

Based on the spectral range and state-of-the art narrow-gap semiconductor technology, Lead Telluride (PbTe) may be selected as the semiconductor material. The following table lists the characteristics of PbTe at $77^{\circ}K$ which is the desirable operating temperature.

E_g = 0.2158 ev

χ = 4.6 volts

n_i = 3.4 X 10^{10} cm^{-3}

κ_s = 400

μ_e = 2 X 10^4 cm^2/volt-sec

μ_n = 1 X 10^4 cm^2/volt-sec

τ_{e_p} = 1 X 10^{-8} sec

τ_{h_n} = 1 X 10^{-7} sec

τ_{GR} = 1 X 10^{-6} sec

ρ_p = 10^{-1} -10 ohm-cm

ρ_n = 10^{-3} -10^{-1} ohm-cm

α = 4000 cm^{-1}

ℓ = 2.7 X 10^{-5} per ^oC

n = 6

Table IV

Since PbTe has a cubic rock salt structure, the <100> orientation should be chosen to reduce surface state density. Although thin film PbTe can be grown, this calculation is for front-side illumination and bulk material will be used. The calculation in the next section for back-side illumination considers thin film PbTe.

b. Insulator

The semiconductor selection of PbTe narrows the choices of insulator material to Ta_2O_5 and TiO_x because of the high dielectric constant of PbTe.

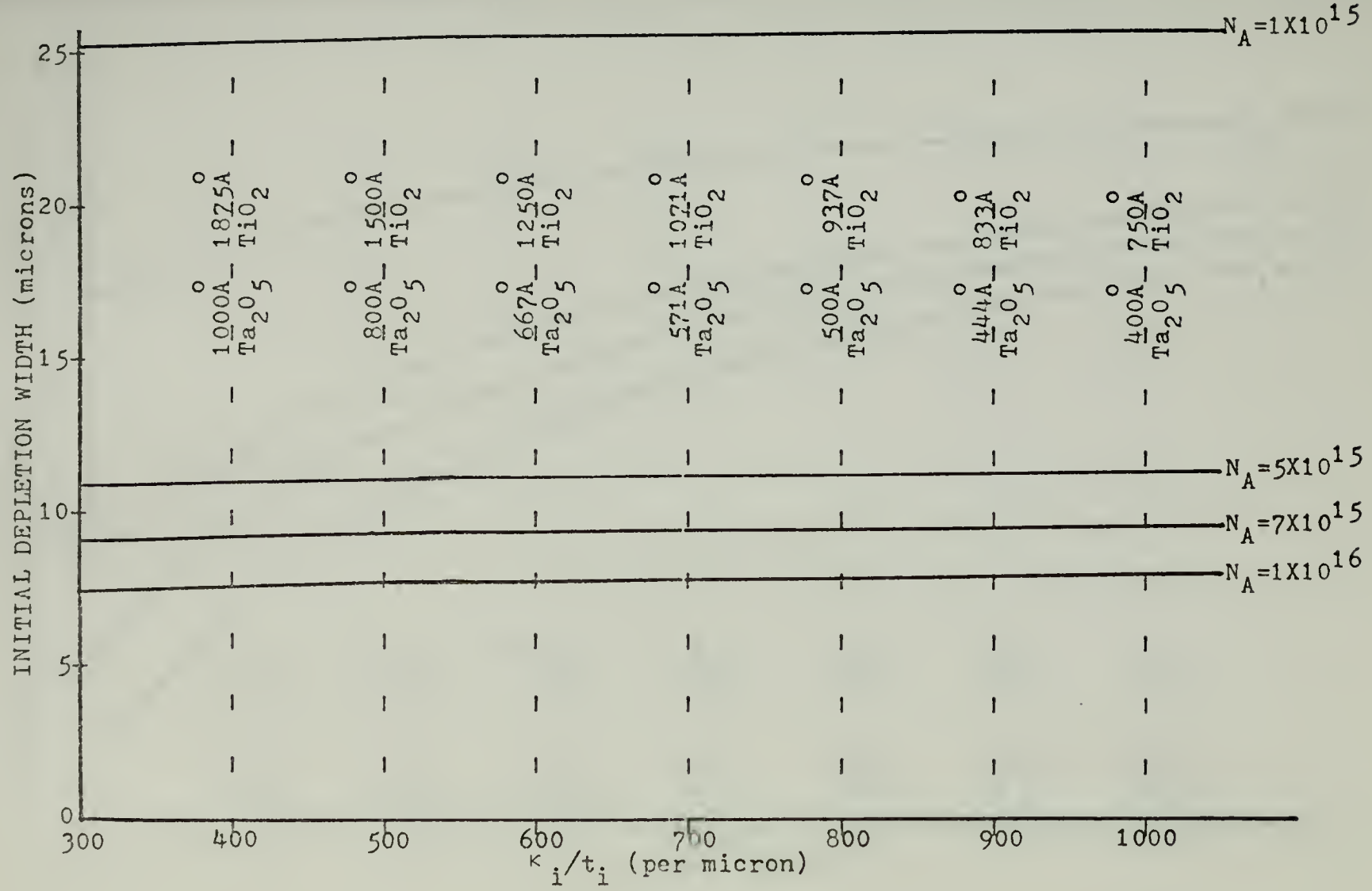

INITIAL DEPLETION WIDTH (microns)
25
20
15
10
5
0
300
400
500
600
700
800
900
1000
κ_i/t_i (per micron)
$N_A=1X10^{15}$
$N_A=5X10^{15}$
$N_A=7X10^{15}$
$N_A=1X10^{16}$
1000Å Ta_2O_5 1825Å TiO_2
800Å Ta_2O_5 1500Å TiO_2
667Å Ta_2O_5 1250Å TiO_2
571Å Ta_2O_5 1071Å TiO_2
500Å Ta_2O_5 937Å TiO_2
444Å Ta_2O_5 833Å TiO_2
400Å Ta_2O_5 750Å TiO_2

Figure 33

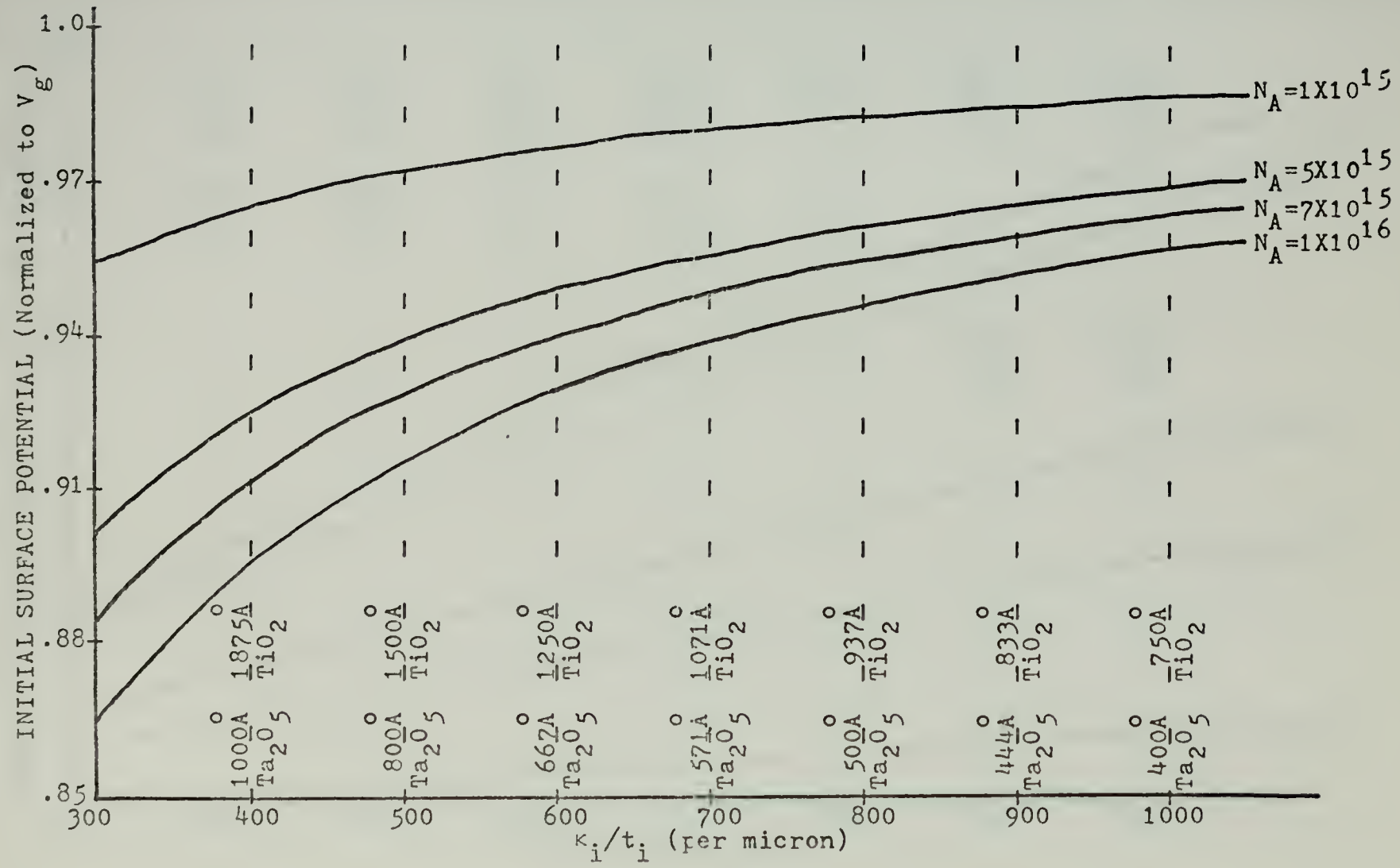

INITIAL SURFACE POTENTIAL (Normalized to V_g)
1.0
.97
.94
.91
.88
.85
300
400
500
600
700
800
900
1000
κ_i/t_i (per micron)
$N_A=1X10^{15}$
$N_A=5X10^{15}$
$N_A=7X10^{15}$
$N_A=1X10^{16}$
1875Å TiO_2 1000Å Ta_2O_5
1500Å TiO_2 800Å Ta_2O_5
1250Å TiO_2 662Å Ta_2O_5
1071Å TiO_2 571Å Ta_2O_5
937Å TiO_2 500Å Ta_2O_5
833Å TiO_2 444Å Ta_2O_5
750Å TiO_2 400Å Ta_2O_5

Figure 34

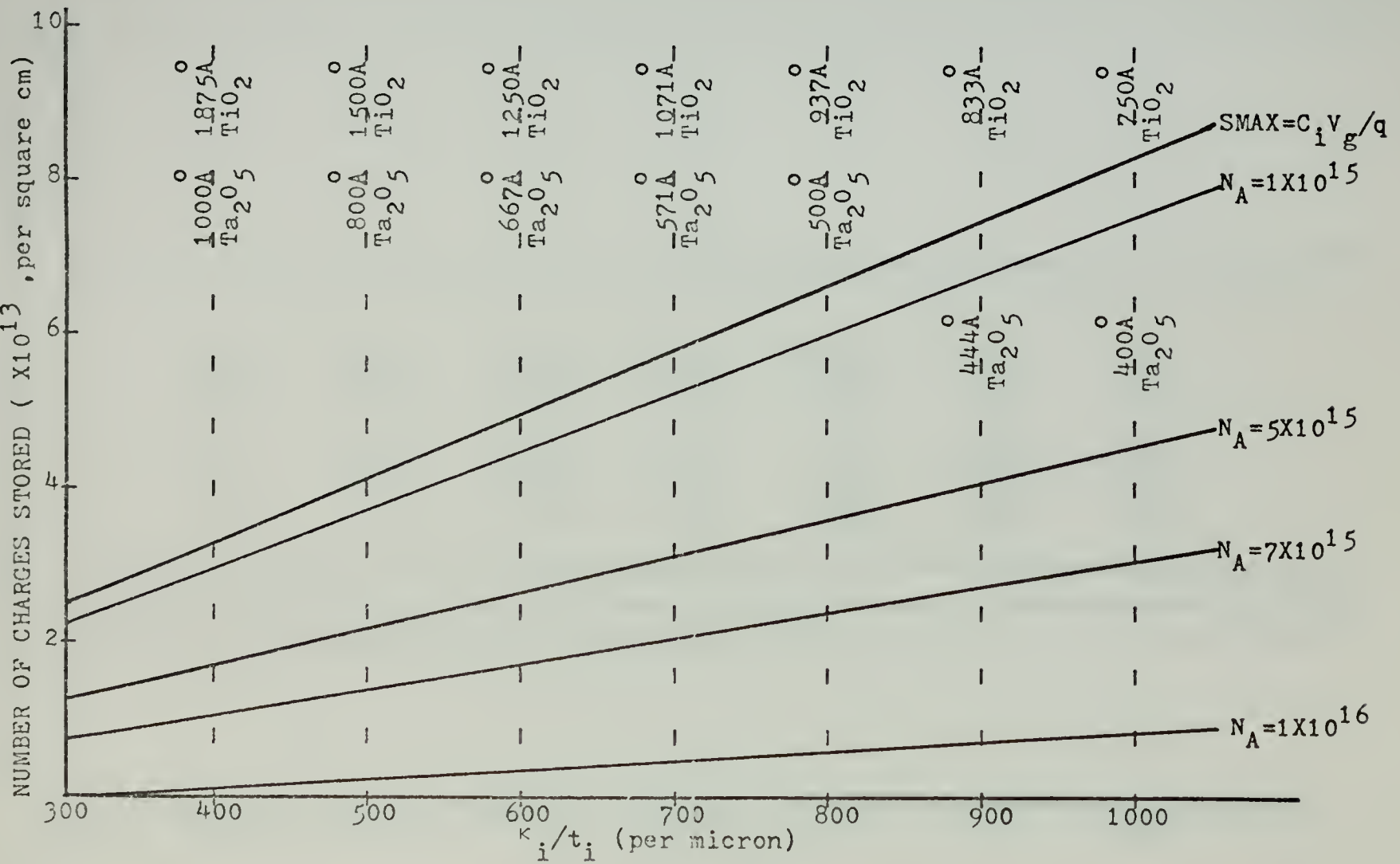

NUMBER OF CHARGES STORED (X10^13 ,per square cm)
10
8
6
4
2
300
400
500
600
700
800
900
1000
K_i/t_i (per micron)
1875A TiO2
1000A Ta2O5
1500A TiO2
800A Ta2O5
1250A TiO2
667A Ta2O5
1071A TiO2
571A Ta2O5
937A TiO2
500A Ta2O5
833A TiO2
444A Ta2O5
750A TiO2
400A Ta2O5
SMAX=C_iV_g/q
N_A=1X10^15
N_A=5X10^15
N_A=7X10^15
N_A=1X10^16

Figure 35

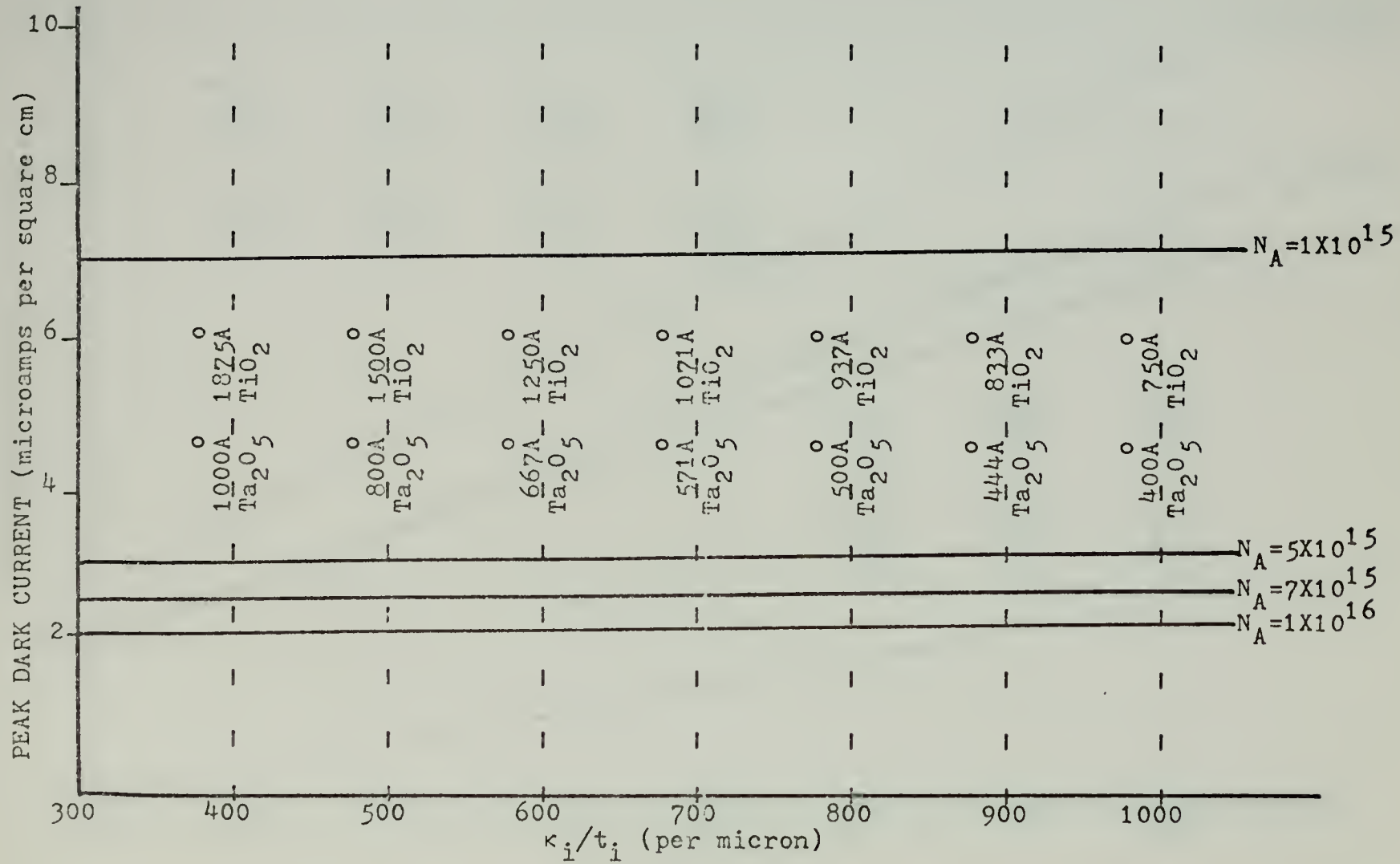

PEAK DARK CURRENT (microamps per square cm)
10
8
6
4
2
300
400
500
600
700
800
900
1000
κ_i/t_i (per micron)
$N_A=1X10^{15}$
$N_A=5X10^{15}$
$N_A=7X10^{15}$
$N_A=1X10^{16}$
1000Å Ta_2O_5 1825Å TiO_2
800Å Ta_2O_5 1500Å TiO_2
667Å Ta_2O_5 1250Å TiO_2
571Å Ta_2O_5 1071Å TiO_2
500Å Ta_2O_5 937Å TiO_2
444Å Ta_2O_5 833Å TiO_2
400Å Ta_2O_5 750Å TiO_2

Figure 36

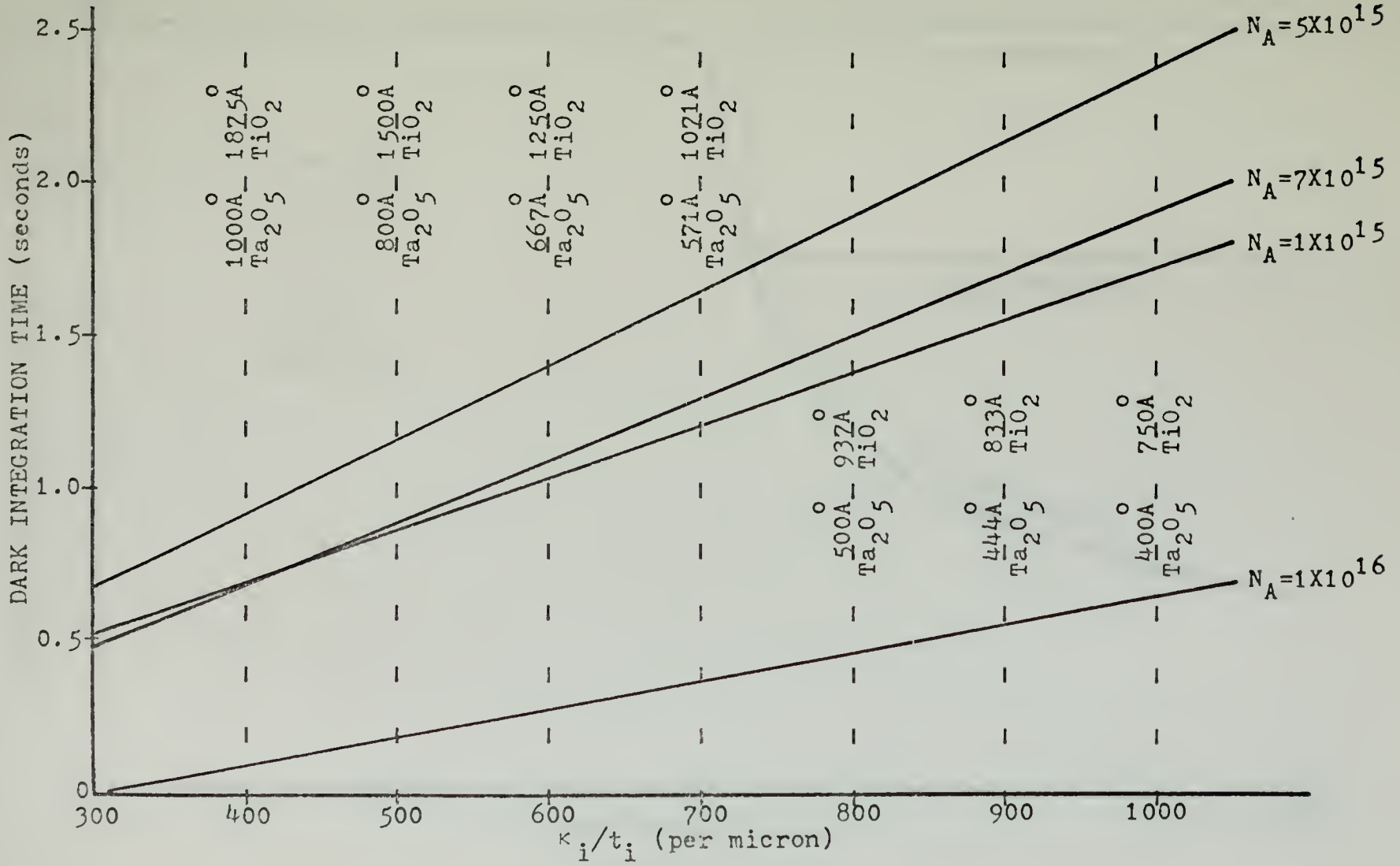

DARK INTEGRATION TIME (seconds)
2.5
2.0
1.5
1.0
0.5
0
300
400
500
600
700
800
900
1000
κ_i/t_i (per micron)
$N_A=5X10^{15}$
$N_A=7X10^{15}$
$N_A=1X10^{15}$
$N_A=1X10^{16}$
1000A Ta_2O_5 1875A TiO_2
800A Ta_2O_5 1500A TiO_2
667A Ta_2O_5 1250A TiO_2
571A Ta_2O_5 1021A TiO_2
500A Ta_2O_5 932A TiO_2
444A Ta_2O_5 833A TiO_2
400A Ta_2O_5 750A TiO_2

Figure 37

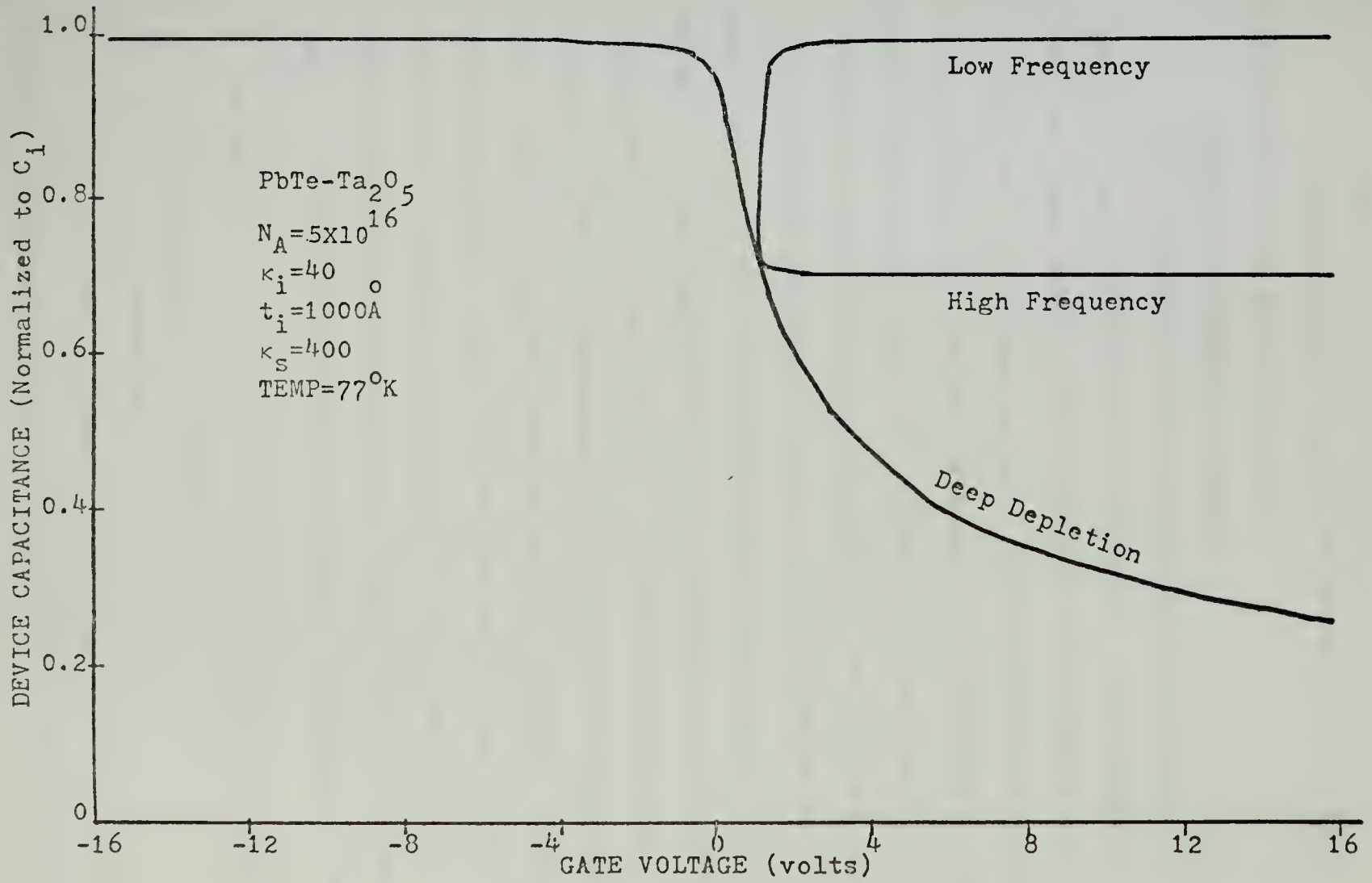
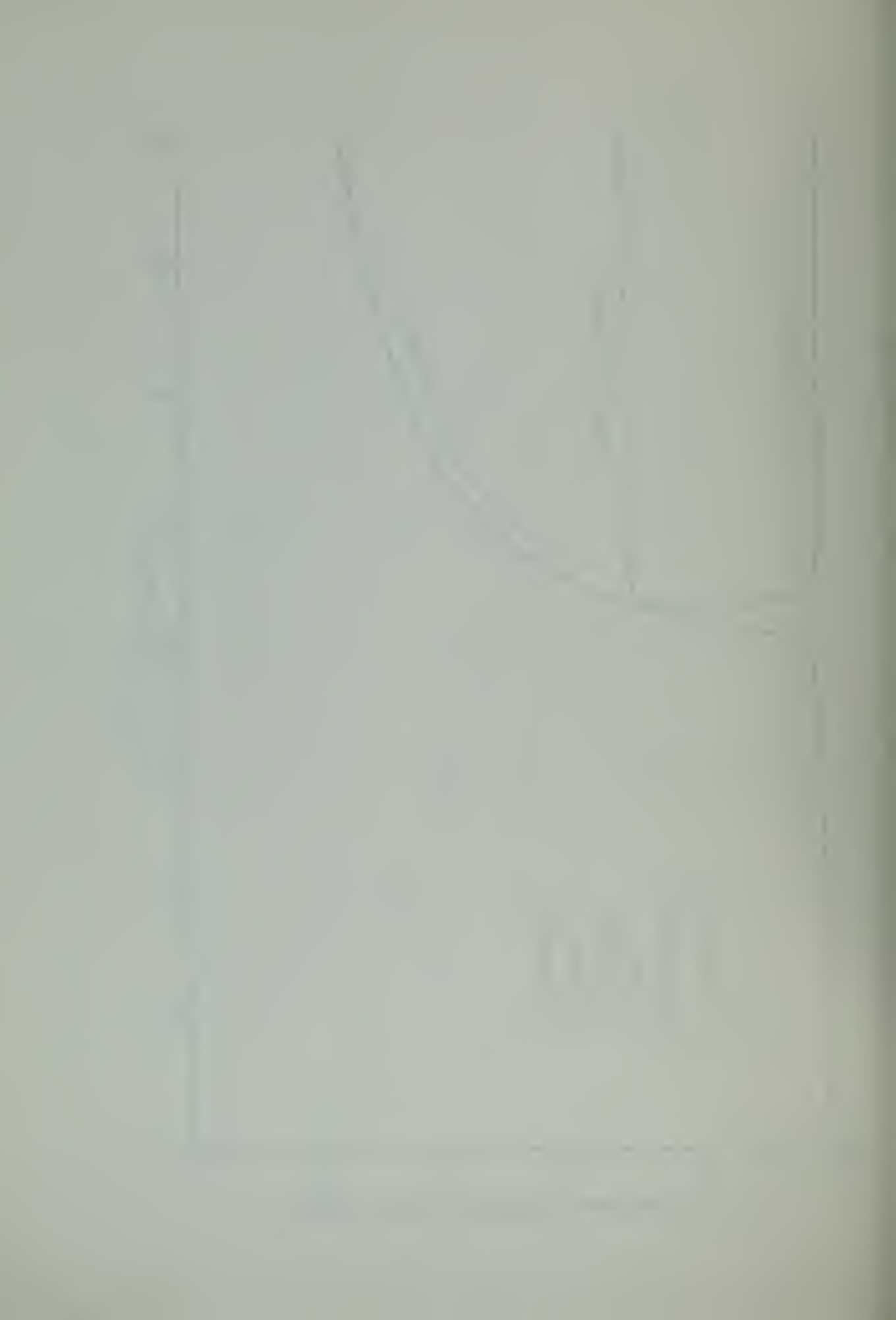

1.0
0.8
0.6
0.4
0.2
0
DEVICE CAPACITANCE (Normalized to C_i)
PbTe-Ta_2O_5
$N_A=5X10^{16}$
$\kappa_i=40$
$t_i=1000A^o$
$\kappa_s=400$
TEMP=77°K
Low Frequency
High Frequency
Deep Depletion
-16
-12
-8
-4
0
4
8
12
16
GATE VOLTAGE (volts)

Figure 38



c. Metal

Since front-illumination is being used, polysilicon gates will be considered.

2. Computer Calculation Results

With slight modifications the computer program in Appendix C was used for this calculation. The resulting plots are shown in Figures 33 through 37 and Figure 38 is the C-V curve of the optimum device. From the computer calculation, it can be seen that low doping levels are desirable. However, doping levels below about $5 \times 10^{16} cm^{-3}$ are not readily available so that value was selected for the optimum device. The calculation indicates that for front-illumination, this doping level is not the optimum but is the present state-of-the-art. Since good quality TiO_2 is probably more difficult to fabricate in large quantity at small thickness than Ta_2O_5 and since the improvement in storage over Ta_2O_5 is not too large, 1000 $\mathring{A}$ Ta_2O_5 was selected as the optimized insulator. This provides for 1.33×10^{12} charges stored per square centimeter. The depletion width is barely deep enough comparing with optical penetration depth to provide good quantum efficiency and the dark current is adequately low.

D. OPTIMIZATION USING THIN FILM PbTe FOR BACK-ILLUMINATION

1. Basic Material Selection

a. Semiconductor

The PbTe parameters are given in the previous section. For back-illumination the semiconductor must be

thin to prevent photons from being absorbed outside of the depletion region. For this reason it is proposed that the gate voltage pulse should be sufficiently high to deplete the entire semiconductor. The understanding of a completely depleted semiconductor is not clear at the present moment but we will consider the case where the initial depletion region occupies nearly all the semiconductor thickness. This requires the thin film PbTe to be on the order of 5 - 10 microns thick which of course depends on the gate voltage and doping level. To reduce surface states, <100> oriented films should be used.

b. Insulator

Again, because of the large dielectric constant of PbTe, Ta_2O_5 and TiO_x are the logical insulator choices.

c. Metal

For back-illumination, transparent gates are not required or even desired. Therefore, the type of metal used for the gates is not crucial except that a good bond to the insulator is required. Au-Ti-Ta_2O_5-PbTe is a good combination which reduces the bonding problems and has been demonstrated to be feasible.

2. Calculation Results

For back-illumination the photon absorption in the bulk is the oposite of the front-illumination case. However, to maintain high quantum efficiencies the difference between the initial and final depletion widths must be kept

within limits determined by the absorption coefficient. Mathematically

$$W_{DEPI} - W_{DEPF} < \frac{\mathcal{Z}}{\alpha}$$

Here it is desirable that $\mathcal{Z}$ be small since the quantum efficiency may be approximated by

$$\eta \simeq (1-R)e^{-\mathcal{Z}}$$

or

$$\eta \simeq (1-R)e^{-\alpha(W_{DEPI}-W_{DEPF})}$$

if W_{DEPI} is approximately equal to the semiconductor thickness. This indicates that if the entire semiconductor thickness can be kept depleted during the charge storage period, the quantum efficiency will be nearly constant at (1-R). Also, a very small $\mathcal{Z}$ means that the charge storage capacity of the device approaches the absolute maximum value of $C_i V_g/q$. Thus, if the previously explained new proposed structure is used, the optimum situation results.

VI. CONCLUSIONS

It is becoming increasingly clear that the emerging charge transport device technology will significantly change surveillance techniques. Specifically, much improvement is anticipated using the added signal processing capabilities at the focal plane when detectors, in either the visible or infrared spectrums, are combined with a CTD signal processor.

This thesis is concerned with the infrared charge transport imager (IRCTI) of which there are two forms. One is hybrid in which the IR detectors are coupled to a silicon CCD signal processor. The other is monolithic in which a CTD array of narrow-gap semiconductor sensitive to infrared radiations is used for both detection and signal processing. This thesis studied the monolithic IRCTI in the 3 to 5.5 micron region. Optimizations were carried out for the design of metal-insulator-semiconductor (M-I-S) structures of bulk crystal InSb and PbTe and thin film PbTe for IRCTI applications.

The important parameters considered in the optimization are highlighted below:

1. Semiconductor

    carrier type
    doping concentrations
    thickness
    dielectric constant

2. Insulator

    dielectric constant
    thickness

3. Operating conditions
    illumination type (front or back)
    clock voltage amplitude
    speed of operation

For all three configurations, recommendations for optimized device design were made and summarized in Table V. However, it was found that of these three cases, the back-illuminated CID using thin film PbTe holds more promise than the other two. Recommendations were given to incorporate as many desirable features as possible for this infrared charge injection imager. Pertinent details can be found in Sections IV. D and V and in Table V.

Table V

	InSb Front-illumination	PbTe Bulk Crystal Front-illumination	PbTe Thin Film Back-illumination
V_g	15	15	15
N_A (per cm^3)	$1X10^{14}$	$5X10^{16}$	$5X10^{16}$
κ_i (Ta_2O_5)	40	40	40
t_i (Angstroms)	1000	1000	1000
Storage (per cm^2)	$2.7X10^{13}$	$1.3X10^{12}$	$3.3X10^{13}$
Dark Current Density ($amps/cm^2$)	$1.4X10^{-5}$	$1.2X10^{-6}$	$1.2X10^{-6}$
Dark Integration Time (sec)	0.31	0.17	4.4
Exposed Integration Time (sec)	$2.7X10^{-3}$	$1.3X10^{-4}$	$3.3X10^{-3}$

APPENDIX A

STORAGE FORMULA DERIVATION

The number of carriers stored in the inversion region during the integration period may be formulated as

$$N = \frac{Q_{INVF} - Q_{INVI}}{q}$$

where Q_{INVF} and Q_{INVI} represent the stored charge at the end and the beginning respectively of the integration time. Q_{INVF} may be found by application of the quantum efficiency constraint boundary condition on W. From figure 14 select a value of $\mathcal{Z} = \alpha W_F$. Then $W_F = \frac{\mathcal{Z}}{\alpha}$ represents the depletion width at the end of the integration period, and

$$\Psi_{S_F} = \frac{q(N_A - N_D)}{2\varepsilon_S} W_F^2$$

but from

$$\Psi_S = V_g - V_{FB} + \frac{Q_{INV}}{C_i} + \frac{Q_{DEP}}{C_i}$$

$$Q_{INV} = (\Psi_S - V_g + V_{FB})\ C_i - Q_{DEP}$$

where

$$Q_{DEP} = -\frac{\varepsilon_S}{W} \Psi_S$$

then

$$Q_{INVF} = (\Psi_{SF} - V_g + V_{FB})\, C_i + \frac{\varepsilon_S}{W}\Psi_S$$

Substitution for Ψ_{SF} and W_F yields

$$Q_{INVI} = \left[\frac{2kT}{q}\ln\left(\frac{|N_A-N_D|}{n_i}\right) - V_g + V_{FB}\right] C_i + \frac{\varepsilon_s\left[2\frac{kT}{q}\ln\left(\frac{|N_A-N_D|}{n_i}\right)\right]}{\left(\frac{2\varepsilon_s}{q(N_A-N_D)}\right)^{1/2}}$$

The minimum charge in the inversion layer, Q_{INVI}, is determined by the equilibrium value of gate voltage just prior to pulsing into the non-equilibrium deep depletion region. If pulsed from accumulation or flat-band $Q_{INVI}=0$. If pulsed from between flat-band and the onset of heavy inversion, $\Psi_S=2\Psi_B$, Q_{INVI} may be found from

$$Q_{INVI} = (\Psi_S - V_g + V_{FB})\, C_i + \frac{\varepsilon_S}{W}\Psi_S$$

and

$$W = \left(\frac{2\varepsilon_S\ \Psi_S}{q(N_A-N_D)}\right)^{1/2}$$

$$\Psi_S = 2\Psi_B = 2\,\frac{kT}{q}\ln\left(\frac{|N_A-N_D|}{n_i}\right)$$

substitution yields

$$Q_{INVI} = \left[2\frac{kT}{q}\ln\left(\frac{|N_A-N_D|}{n_i}\right) - V_g + V_{FB}\right] C_i + \frac{\varepsilon_s\left[2\frac{kT}{q}\ln\left(\frac{|N_A-N_D|}{n_i}\right)\right]}{\left(\frac{2\varepsilon_s}{q(N_A-N_D)}\right)^{1/2}}$$

If pulsed from heavy inversion

$$Q_{INVI} = (\Psi_S - V_g + V_{FB})\ C_i + \frac{\varepsilon_S}{W}\ \Psi_S$$

which must be solved for using the proper values of Ψ_S and W. However the further the device is biased into heavy inversion before the depletion pulse is applied the nearer Q_{INVI} will approach $C_i V_g$ and the storage capability is drastically reduced.

The non-ideal situation can be handled simply by substitution of

$$\frac{Q_{SS} + Q_{fc}}{C_i} + \phi_{MS}$$

for V_{FB} wherever appearing in the ideal formulation if Q_{SS} and Q_{fc} are assumed to be nearly constant.

```
      DIMENSION X1(100),Y1(100),Y2(100),Y3(100),Y4(100),Y5(100),Y6(100),
     1Y7(100),Y8(100)
      REAL KS,KINS,NA,ND
      REAL LABL1/'Z=1.'/
      REAL LABL2/'Z=2.'/
      REAL LABL3/'Z=3.'/
      REAL LABL4/' S2 '/
      REAL LABL5/' S3 '/
      REAL LABL6/' S4 '/
      REAL LABL7/'SMAX'/
      REAL*8 TITLE(12)
      KS=18.0
      TEMP=77.0
      KINS=40.
      TINS=0.1E-04
      VFB=0.0
      CINT=1.0E10
      ALPHA=4000.
      BOLTZ=1.38E-23
      Q=1.6E-19
      EZERO=8.854E-14
 1000 INDEX=0
      EINS=KINS*EZERO
      ES=KS*EZERO
      CINS=EINS/TINS
      VG=15.
      DOPE=5.E12
      ND=0.0
      SMAX=CINS*VG/Q
 1500 INDEX=INDEX+1
      Z=1.
      MM=0
 2000 CONTINUE
      MM=MM+1
      NA=DOPE
      DUMMY=ES/(2.*CINS)
      WDEPI=SQRT((VG-VFB)*2.*ES/(Q*(NA-ND))+DUMMY**2)-DUMMY
      TEST=Z/ALPHA
      IF (WDEPI.LT.TEST) GO TO 2050
      DUMMY1=(Q*(NA-ND)*CINS/(2.*ES))*((Z/ALPHA)**2)
      DUMMY2=(VG-VFB)*CINS
      DUMMY3=Q*(NA-ND)*Z/(2.*ALPHA)
      QINVF=DUMMY1-DUMMY2+DUMMY3
      S1=ABS(QINVF/Q)/SMAX
      GO TO 2051
 2050 S1=0.
 2051 CONTINUE
      IF(MM.EQ.1) GO TO 2100
```

```
      IF(MM.EQ.2) GO TO 2200
      IF(MM.EQ.3) GO TO 2300
2100  Y1(INDEX)=S1
      Z=2.
      GO TO 2000
2200  Y2(INDEX)=S1
      Z=3.
      GO TO 2000
2300  Y3(INDEX)=S1
      BETA=Q*ES*DOPE/CINS
      CDD=CINS/SQRT(1.+2.*CINS*(VG-VFB)/BETA)
      S2=((CINS-CDD)*ABS(VG-VFB))/(Q*SMAX)
      PHIB=BOLTZ*TEMP*ALOG(ABS(NA-ND)/CINT)/Q
      WTH=SQRT(4.*ES*PHIB/(Q*(NA-ND)))
      CMIN=EINS/(TINS+(EINS/ES)*WTH)
      VTH=2.*PHIB/(1.-CMIN/CINS)
      S3=CINS*(VG-VTH)/(Q*SMAX)
      WHF=SQRT(4.*ES*BOLTZ*TEMP*ALOG(DOPE/CINT)/(DOPE*Q**2))
      CHF=(EINS/(TINS+WHF*EINS/ES))
      S4=((CHF-CDD)*(VG-VFB))/(Q*SMAX)
      XAXIS=ALOG10(DOPE)-12.5
      X1(INDEX)=XAXIS
      Y4(INDEX)=S2
      Y5(INDEX)=S3
      Y6(INDEX)=S4
      Y7(INDEX)=1.
      DOPE=DOPE*1.2
      IF (INDEX.EQ.42) GO TO 5000
      GO TO 1500
5000  READ(5,5001)TITLE
5001  FORMAT(6A8)
      CALL DRAW(INDEX,X1,Y1,1,0,LABL1,TITLE,0.5,0.2,0,0,0,0,8,6,0,LAST)
      CALL DRAW(INDEX,X1,Y2,2,0,LABL2,TITLE,0,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,Y3,2,0,LABL3,TITLE,0,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,Y4,2,0,LABL4,TITLE,0,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,Y5,2,0,LABL5,TITLE,0,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,Y6,2,0,LABL6,TITLE,0,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,Y7,3,0,LABL7,TITLE,0,0,0,0,0,0,0,0,0,LAST)
      END
```

```
      DIMENSION W1(100),W2(100),W3(100),W4(100),W5(100),W6(100),W7(100),
     1W8(100),W9(100)
      DIMENSION P1(100),P2(100),P3(100),P4(100),P5(100),P6(100),P7(100),
     1P8(100),P9(100)
      DIMENSION S1(100),S2(100),S3(100),S4(100),S5(100),S6(100),S7(100),
     1S8(100),S9(100)
      DIMENSION J1(100),J2(100),J3(100),J4(100),J5(100),J6(100),J7(100),
     1J8(100),J9(100)
      DIMENSION T1(100),T2(100),T3(100),T4(100),T5(100),T6(100),T7(100),
     1T8(100),T9(100)
      DIMENSION X1(100),SX(100)
       REAL KS,NA,ND,MINMOB,NI,JGD,JGB,JDARK,J1,J2,J3,J4,J5,J6,J7,J8,J9
      REAL LABL1/'1E13'/
      REAL LABL2/'3E13'/
      REAL LABL3/'5E13'/
      REAL LABL4/'7E13'/
      REAL LABL5/'1E14'/
      REAL LABL6/'3E14'/
      REAL LABLX/'SMAX'/
      REAL*8 TITLE(12)
      Q=1.6E-19
      EZERO=8.854E-14
      BOLTZ=1.38E-23
      TAUGR=1.E-07
      KS=18.
      NI=1.E10
      TEMP=77.
      MINMOB=1.E04
      TAUMIN=2.E-10
      ALPHA=4000.
      Z=3.
      VFB=0.
      VG=15.
      ES=KS*EZERO
      WRITE(6,1001)
1001 FORMAT('1',2X,9HINSULATOR3X,13HSEMICONDUCTOR3X,7HINITIAL3X,7HINITI
     1AL3X,9HNUMBER OF4X,4HDARK7X,4HDARK)
      WRITE(6,1002)
1002 FORMAT(1X,11HCAPACITANCE5X,6HDOPING6X,9HDEPLETION3X,7HSURFACE4X,6H
     1STORED4X,7HCURRENT3X,11HINTEGRATION)
      WRITE(6,1003)
1003 FORMAT(18X,5HLEVEL8X,5HWIDTH4X,9HPOTENTIAL2X,8HCARRIERS4X,5H(AMPS7
     1X,4HTIME)
      WRITE(6,1004)
1004 FORMAT(2X,9H(FAR/CM2)5X,9H(PER CM3)6X,4H(CM)6X,7H(VOLTS)3X,9H(PER
     1CM2)2X,8HPER CM2)4X,6H(SECS))
1300 CONTINUE
      XAXIS=5.
```

```
      INDEX=1
1400  LL=0
      CINS=XAXIS*1.E04*EZERO
      DOPE=1.E13
      ND=0.
1500  LL=LL+1
      NA=DOPE
2000  DUMMY=ES/(2.*CINS)
      WDEPI=SQRT((VG-VFB)*2.*ES/(Q*(NA-ND))+DUMMY**2)-DUMMY
      PHISI=Q*(NA-ND)*(WDEPI**2)/(2.*ES)
      DUMMY1=(Q*(NA-ND)*CINS/(2.*ES))*((Z/ALPHA)**2)
      DUMMY2=(VG-VFB)*CINS
      DUMMY3=Q*(NA-ND)*Z/(2.*ALPHA)
      QINVF=DUMMY1-DUMMY2+DUMMY3
      STORE=ABS(QINVF/Q)
      TEST=Z/ALPHA
      IF (WDEPI.LT.TEST) GO TO 2100
      GO TO 2200
2100  WRITE(6,2150)
2150  FORMAT(90H********************************* DEPLETION WIDTH OUT OF RA
     1NGE *********************************)
2200  SMAX=CINS*VG/Q
      JGD=Q*NI*WDEPI/(2.*TAUGR)
      JGB=Q*(NI**2)*SQRT(MINMOB*BOLTZ*TEMP*TAUMIN/Q)/(TAUMIN*ABS(NA-ND))
      JDARK=JGB+JGD
      TAUID=Q*STORE/JDARK
      WRITE(6,2500) CINS,DOPE,WDEPI,PHISI,STORE,JDARK,TAUID
2500  FORMAT(1X,1PE10.2,5X,E10.2,2X,E10.2,4X,0PF4.1,4X,1P2E10.2,2X,E10.2
     1)
3000  IF (LL.EQ.1) GO TO 4001
      IF (LL.EQ.2) GO TO 4002
      IF (LL.EQ.3) GO TO 4003
      IF (LL.EQ.4) GO TO 4004
      IF (LL.EQ.5) GO TO 4005
      IF (LL.EQ.6) GO TO 4006
4001  W1(INDEX)=WDEPI
      P1(INDEX)=PHISI-12.5
      S1(INDEX)=STORE
      J1(INDEX)=JDARK
      T1(INDEX)=TAUID
      DOPE=3.E13
      GO TO 1500
4002  W2(INDEX)=WDEPI
      P2(INDEX)=PHISI-12.5
      S2(INDEX)=STORE
      J2(INDEX)=JDARK
      T2(INDEX)=TAUID
      DOPE=5.E13
```

```
      GO TO 1500
4003  W3(INDEX)=WDEPI
      P3(INDEX)=PHISI-12.5
      S3(INDEX)=STORE
      J3(INDEX)=JDARK
      T3(INDEX)=TAUID
      DOPE=7.E13
      GO TO 1500
4004  W4(INDEX)=WDEPI
      P4(INDEX)=PHISI-12.5
      S4(INDEX)=STORE
      J4(INDEX)=JDARK
      T4(INDEX)=TAUID
      DOPE=1.E14
      GO TO 1500
4005  W5(INDEX)=WDEPI
      P5(INDEX)=PHISI-12.5
      S5(INDEX)=STORE
      J5(INDEX)=JDARK
      T5(INDEX)=TAUID
      DOPE=3.E14
      GO TO 1500
4006  W6(INDEX)=WDEPI
      P6(INDEX)=PHISI-12.5
      S6(INDEX)=STORE
      J6(INDEX)=JDARK
      T6(INDEX)=TAUID
      SX(INDEX)=SMAX
      X1(INDEX)=XAXIS
      XAXIS=XAXIS+10.
      IF (XAXIS.GT.750.) GO TO 5000
      INDEX=INDEX+1
      WRITE(6,4500)
4500  FORMAT('0')
      GO TO 1400
5000  CONTINUE
5100  CONTINUE
      READ(5,5200)TITLE
5200  FORMAT(6A8)
      CALL DRAW(INDEX,X1,W1,1,0,LABL1,TITLE,100.,1.E-03,0,0,0,0,8,6,0,LA
     1ST)
      CALL DRAW(INDEX,X1,W2,2,0,LABL2,TITLE,0,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,W3,2,0,LABL3,TITLE,0,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,W4,2,0,LABL4,TITLE,0,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,W5,2,0,LABL5,TITLE,0,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,W6,3,0,LABL6,TITLE,0,0,0,0,0,0,0,0,0,LAST)
      READ(5,5200)TITLE
      CALL DRAW(INDEX,X1,P1,1,0,LABL1,TITLE,100.,.5,0,0,0,0,8,6,0,LAST)
```

```
      CALL DRAW(INDEX,X1,P2,2,0,LABL2,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,P3,2,0,LABL3,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,P4,2,0,LABL4,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,P5,2,0,LABL5,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,P6,3,0,LABL6,TITLE,0,0,0,0,0,0,0,0,LAST)
      READ(5,5200)TITLE
      CALL DRAW(INDEX,X1,S1,1,0,LABL1,TITLE,100.,1.E13,0,0,0,0,8,6,0,LAS
     1T)
      CALL DRAW(INDEX,X1,S2,2,0,LABL2,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,S3,2,0,LABL3,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,S4,2,0,LABL4,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,S5,2,0,LABL5,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,S6,2,0,LABL6,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,SX,3,0,LABLX,TITLE,0,0,0,0,0,0,0,0,LAST)
      READ(5,5200)TITLE
      CALL DRAW(INDEX,X1,J1,1,0,LABL1,TITLE,100.,2.0E-06,0,0,0,0,8,6,0,L
     1AST)
      CALL DRAW(INDEX,X1,J2,2,0,LABL2,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,J3,2,0,LABL3,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,J4,2,0,LABL4,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,J5,2,0,LABL5,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,J6,3,0,LABL6,TITLE,0,0,0,0,0,0,0,0,LAST)
      READ(5,5200)TITLE
      CALL DRAW(INDEX,X1,T1,1,0,LABL1,TITLE,100.,0.1,0,0,0,0,8,6,0,LAST)
      CALL DRAW(INDEX,X1,T2,2,0,LABL2,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,T3,2,0,LABL3,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,T4,2,0,LABL4,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,T5,2,0,LABL5,TITLE,0,0,0,0,0,0,0,0,LAST)
      CALL DRAW(INDEX,X1,T6,3,0,LABL6,TITLE,0,0,0,0,0,0,0,0,LAST)
 9000 CONTINUE
      END
```

INSULATOR CAPACITANCE (FAR/CM2)	SEMICONDUCTOR DOPING LEVEL (PER CM3)	INITIAL DEPLETION WIDTH (CM)	INITIAL SURFACE POTENTIAL (VOLTS)	NUMBER OF STORED CARRIERS (PER CM2)	DARK CURRENT (AMPS PER CM2)	DARK INTEGRATION TIME (SECS)
4.43E-09	1.00E 13	5.29E-03	14.0	4.03E 11	4.32E-05	1.49E-03
4.43E-09	3.00E 13	2.98E-03	13.4	3.80E 11	2.42E-05	2.52E-03
4.43E-09	5.00E 13	2.27E-03	12.9	3.57E 11	1.84E-05	3.11E-03
4.43E-09	7.00E 13	1.89E-03	12.6	3.34E 11	1.53E-05	3.50E-03
4.43E-09	1.00E 14	1.56E-03	12.2	2.99E 11	1.26E-05	3.82E-03
4.43E-09	3.00E 14	8.34E-04	10.5	6.82E 10	6.70E-06	1.63E-03
1.33E-08	1.00E 13	5.41E-03	14.7	1.22E 12	4.42E-05	4.41E-03
1.33E-08	3.00E 13	3.10E-03	14.4	1.16E 12	2.51E-05	7.42E-03
1.33E-08	5.00E 13	2.39E-03	14.3	1.11E 12	1.93E-05	9.21E-03
1.33E-08	7.00E 13	2.01E-03	14.2	1.05E 12	1.62E-05	1.04E-02
1.33E-08	1.00E 14	1.67E-03	14.0	9.73E 11	1.34E-05	1.16E-02
1.33E-08	3.00E 14	9.40E-04	13.3	4.29E 11	7.55E-06	9.10E-03
2.21E-08	1.00E 13	5.43E-03	14.8	2.03E 12	4.44E-05	7.33E-03
2.21E-08	3.00E 13	3.12E-03	14.7	1.95E 12	2.53E-05	1.23E-02
2.21E-08	5.00E 13	2.41E-03	14.6	1.86E 12	1.95E-05	1.53E-02
2.21E-08	7.00E 13	2.03E-03	14.5	1.78E 12	1.64E-05	1.73E-02
2.21E-08	1.00E 14	1.69E-03	14.4	1.65E 12	1.36E-05	1.93E-02
2.21E-08	3.00E 14	9.63E-04	14.0	7.91E 11	7.73E-06	1.64E-02
3.10E-08	1.00E 13	5.44E-03	14.9	2.85E 12	4.44E-05	1.02E-02
3.10E-08	3.00E 13	3.13E-03	14.8	2.73E 12	2.54E-05	1.72E-02
3.10E-08	5.00E 13	2.42E-03	14.7	2.61E 12	1.95E-05	2.14E-02
3.10E-08	7.00E 13	2.04E-03	14.6	2.50E 12	1.65E-05	2.43E-02
3.10E-08	1.00E 14	1.70E-03	14.6	2.32E 12	1.37E-05	2.71E-02
3.10E-08	3.00E 14	9.73E-04	14.2	1.15E 12	7.81E-06	2.30E-02
3.98E-08	1.00E 13	5.45E-03	14.9	3.66E 12	4.45E-05	1.32E-02
3.98E-08	3.00E 13	3.14E-03	14.8	3.51E 12	2.54E-05	2.21E-02
3.98E-08	5.00E 13	2.42E-03	14.8	3.36E 12	1.96E-05	2.75E-02
3.98E-08	7.00E 13	2.05E-03	14.7	3.22E 12	1.65E-05	3.12E-02
3.98E-08	1.00E 14	1.71E-03	14.7	2.99E 12	1.38E-05	3.48E-02
3.98E-08	3.00E 14	9.78E-04	14.4	1.51E 12	7.86E-06	3.08E-02

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c.1 Design optimization of metal-insulator-semi-conductor devices for infrared solid state imaging.
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